Time-to-Digital Converter Using a Tuned-Delay Line Evaluated in 28-, 40-, and 45-nm FPGAs

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***Abstract*— This paper proposes a bin-width tuning method for a field-programmable gate array (FPGA)-based delay line for a time-to-digital converter (TDC). Changing the hit transitions and sampling patterns of the carry chain considering delays of the sum and carry-out bins can improve the bin-width uniformity and thus measurement precision. The proposed sampling method was evaluated and compared with the ordinary tapped-delay-line (TDL) method in three different types of FPGAs: Kintex-7, Virtex-6, and Spartan-6. The linearity, equivalent bin width, and measurement precision improved for all the evaluated FPGAs by adopting the proposed method. The measurement precision obtained using the simple TDL architecture is comparable with other complex TDC architectures. In addition, the proposed method improves bin-width uniformity and measurement precision while maintaining the advantages of TDL TDCs, that is, fast conversion rate and small resource usage. Furthermore, the enhanced linearity of the delay line can also improve other carry-chain-based FPGA-TDCs.**

***Index Terms*— Bin width, carry chain, equivalent bin width, field-programmable gate array (FPGA), measurement uncertainty, nonlinearity, quantization error, tapped-delay line (TDL), time measurement, time-to-digital converter (TDC), tuning.**

I. Introduction

TIME-TO-DIGITAL converters (TDCs) have been developed to meet the needs of precise time measurement: time-of-flight (TOF) detector [1], time-of-propagation detector [2], light detection and ranging [3], ultrawideband radio frequency localization [4], [5], all digital phase-locked loop (PLL) [6], time-domain analog-to-digital converter [7], time-over-threshold [8], [9], positron emission tomography (PET) [10]–[12], TOF PET [13]–[19], time-based multiplexing [20], and time-resolved fluorescence spectroscopy [21], [22]. Fully digital TDCs implemented in an application-specific integrated chip (ASIC) and a field-programmable gate array (FPGA) offer fast conversion rates and robustness to external disturbances [23]. Most integrated TDCs use a coarse-fine architecture to obtain both wide dynamic range and fine resolution. A digital delay line is used as a fine-time interpolator to achieve fine time resolution. The delay line consists of several delay bins (i.e., quantization steps); finer and more uniform bin widths can lower the quantization error. The bin widths of ASIC-TDCs can be adjusted or linearized using voltage-controlled delay cells and a delay-locked loop [24]–[26]. However, in FPGA-TDCs, the innate propagation time of a delay element determines the bin width.

Although the FPGA-TDC suffers from innate high nonlinearity, it has the advantages of faster development times and lower development costs than the ASIC-TDC. Thus, FPGA-TDCs are widely used, and many TDC architectures have been developed to mitigate nonlinearity and measurement uncertainty. Bin decimation (also known as downsampling) reduces the number of sampling bins of the delay element [27]. Although this method improves linearity, it decreases the resolution [least significant bit (LSB)]. A multidelay-line TDC, where each TDC channel has several delay lines, the delay bins of which subdivide each other, can obtain finer resolution, but this requires more FPGA resource usage [28], [29]. The cyclic or multitime measurement method using a ring oscillator can also achieve finer resolution, but demands longer sampling clock cycles, and thus decreases the conversion rate [30]–[32]. A vernier delay line uses delay differences of the delay elements to obtain subgate-delay bin widths; however, careful placement and routing constraints should be considered when this is implemented in an FPGA [33]. A novel method of a wave-union TDC significantly reduces the bin width and uncertainty, but can increase dead time and require a difficult and complex fine-code encoding scheme [34]–[36].

In this paper, we propose a bin-width tuning method and implemented a tapped-delay-line (TDL) TDC using a tuned delay line, where the TDL TDC is superior with respect to conversion rate, resource usage, and ease of encoding [27], [37]–[40]. The proposed architecture can reduce nonlinearity, equivalent bin width [28], [41] (or equivalent resolution [29], [42]), and measurement uncertainty while maintaining its strengths of fast conversion rate and small resource usage (i.e., multichannel extension capability), and we verified that the proposed method improved the TDC performance compared with the ordinary TDL TDC for a variety of FPGA devices: Kintex-7 (KC705, XC7K325T-2FFG900C, Xilinx), Virtex-6 (ML605, XC6VLX240T-1FFG1156, Xilinx), and Spartan-6 (SP605, XC6SLX45T-FGG484-3C, Xilinx).

II. Design

A. Carry Element

Most FPGAs consist of an array of configurable logic blocks (CLBs) containing memory elements (e.g., flip-flop),

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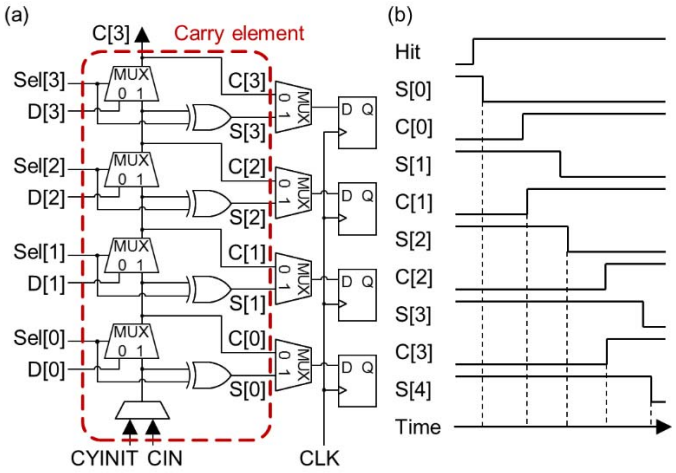

Fig. 1. (a) Simplified CLB structure. (b) Timing diagram of the carry element. The Sels and Data (D) are driven to the logical high and low, respectively. The carry cascade input (CIN) is connected to the last C of the previous carry element. S[4] indicates the first S of the next carry element. There are eight flip-flops in each CLB; however, only four flip-flops can drive carry element outputs of the same CLB directly. The other four flip-flops are omitted.

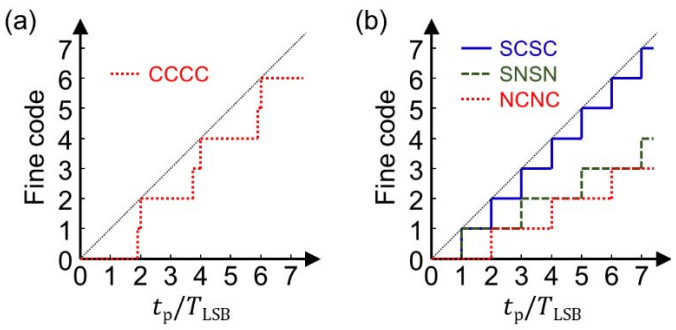

Fig. 2. (a) Transfer function of the homogeneous sampling TDC. (b) Transfer function of the heterogeneous sampling TDC. The x-axis t_p/T_{LSB} is the normalized propagation time. The y-axis fine code indicates the number of flipped delay elements. The sampling patterns are noted.

combinational elements [i.e., lookup tables (LUTs)], and carry elements. The carry element is a hard-wired component for fast arithmetic calculation, and thus, the propagation delay is short and each carry element can be cascaded to the next one. A carry chain (i.e., cascaded carry elements) calculates sums (S) and carry-outs (C) from the LSB to the most significant bit asynchronously and either Ss or Cs are sampled by flip-flops at the rising time of the clock signal CLK.

In an FPGA-TDC, the carry chain can be used as a digital delay line that measures the fine time (i.e., time difference between the asynchronous hit arrival time and rising time of CLK) with subclock-period resolution [27]–[31], [34]–[40]. As shown in Fig. 1(a), the evaluated FPGAs have the same CLB structure, including the carry element, and each carry element has four Ss and four Cs, which are available for delay-line implementation. When the carry-mux select lines (Sel) are driven to the logical high, the asynchronous hit transition fed through the carry-in initialization input (CYINIT) can propagate along the carry chain while flipping the logical states of the Ss and Cs, as shown in Fig. 1(b). The hit transitions can be 0-to-1 or 1-to-0. The fine time is obtained from the numbers of flipped carry element outputs at the rising time of CLK. Note that the S and C have opposite logical states.

In a practical hardware implementation, only four of the total eight carry element outputs (i.e., four Ss and four Cs) can be directly routed to the flip-flops in the same CLB. In the case where output is routed to the flip-flop of another CLB, the trace from the carry element output to the flip-flop and thus bin width becomes unexpected. Thus, a maximum of four outputs are usually used [37], [38], [40], yielding 16 ($=2^4$) different sampling patterns; either S or C can be selected individually as the output.

B. Heterogeneous Sampling TDC

The ordinary design employs the same type of outputs, either S or C. However, there are some known problems deteriorating linearity: several missing bins (i.e., bin width of zero) and alternate wide and narrow bins [27], [37]–[40]. The transfer function is also highly nonlinear, as shown in Fig. 2(a).

The proposed method involves tuning bin widths to be uniform by changing the sampling pattern of a carry element, where sampling pattern indicates the carry element output connected to the flip-flop. Because sampling missing bins deteriorates bin-width uniformity, linearity can be improved by replacing the carry element output corresponding to the missing bin with the other type of output corresponding to a nonmissing bin. This replaced bin not only involves quantization but also divides a wide bin, thereby improving the bin width uniformity. For example, in the case where consecutive S or C bins are alternately wide and narrow (and often missing), as shown in Figs. 1(b) and 2(a), replacing every second and fourth S bins with C bins provides better linearity and a lower quantization error, as shown in Fig. 2(b), e.g., replacing S[1] and S[3] with C[1] and C[3], respectively. The details are discussed in Section IV-A.

Hereafter, we refer to this proposed design that can tune bin widths using both S and C as heterogeneous sampling and the ordinary one that employs the same type of carry element output as homogeneous sampling. We also represent the sampling pattern as an abbreviation, such as SCSC, SCSS, or SCCC, where S, C, and N indicate sum, carry-out, and none, respectively.

C. Architecture

As shown in Fig. 3, the developed TDC employs a coarse-fine architecture and measures hit arrival times t_{A} as follows:

$$t_A = N_{\mathrm{coarse}} \times T_0 - f. \tag{1}$$

In (1), N_{coarse}, T_0, and f denote the coarse count, clock period, and fine time (i.e., subclock-period time between the asynchronous hit arrival time and rising time of CLK), respectively. The PLL or mixed-mode clock manager (MMCM) synthesizes a 400-MHz reference CLK, which drives the coarse counter, sampling flip-flops of the delay line, and other auxiliary modules. The coarse counter measures t_A with a clock period resolution T_0 of 2.5 ns and yields N_{coarse}. The fine-time interpolator measures f and includes a TDL and fine-code encoder. An asynchronous hit signal is delayed while flipping the logical states of the delay elements until it synchronizes with

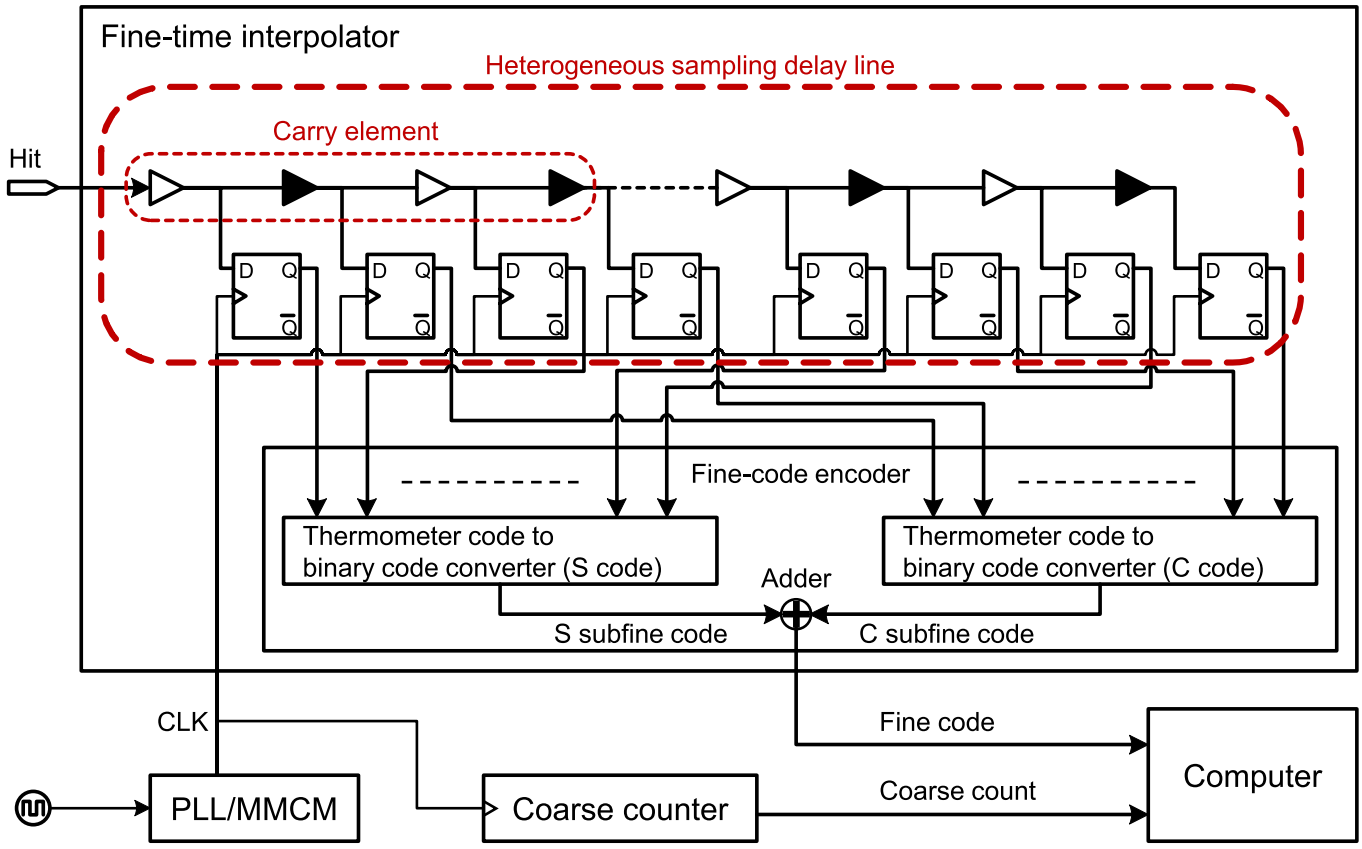

Fig. 3. Architecture of the heterogeneous sampling TDC.

the CLK, and then, the logical states of the delay elements are sampled by flip-flops of the delay line, where f is proportional to the number of flipped logical states. The flip-flop synchronizer follows the sampling flip-flops to avoid a metastable state [43]. The delay line can be either homogeneous or heterogeneous. The lengths of the delay line are 300 bins for Kintex-7 and Virtex-6 and 160 bins for Spartan-6; delay lines are designed, such that the dynamic range of the fine-time interpolator is longer than one clock period. The fine-code encoder converts the thermometer codes (sampled states of the delay line) into binary codes (i.e., fine codes) indicating the number of flipped delay elements in two consecutive steps. The first step applies a bubble error corrector, which converts the thermometer codes (e.g., 1110000...) into one-hot codes (e.g., 001000...) [44], while the second step invokes a fat tree encoder, which converts the one-hot codes to binary codes.

For a heterogeneous sampling delay line, the S and C bins are encoded into S subfine code and C subfine code individually, and then summed to obtain a single fine code, as shown in Fig. 3. This method needs two separate thermometer code to binary code converters, but the total resource usage of the fine-code encoder is not much different from that of the homogeneous sampling TDC. This is because each converter covers a different fraction of the delay line and the binary adder uses minimal resources. For example, a single 300-b thermometer code to 9-b binary code converter was used for the homogeneous sampling TDCs implemented in Kintex-7, while two 150-b thermometer code to 8-b binary code converters and an 8-b adder were used for the heterogeneous ones.

Nonlinearity can be calibrated either online using the FPGA [29], [40], [44] or offline using the computer [38]. To exploit raw fine codes fully for analysis, the coarse count and fine code were transmitted to the computer without calibration. The calibration procedure using a code density test, a statistical method estimating every bin width, was carried out in the computer. When the random hit signals are fed into a fine-time interpolator, the portion of the number of collected hit signals into each fine code to the total number of hit signals is the same as the portion of the respective bin width to the clock period [44]. From the known T_0 and total number of hit signals H_{total} and the measured number of hit signals collected into the ith bin H_i, the ith bin width w_i was obtained using $w_i = (H_i/H_{\text{total}}) \times T_0$, and then, the ith fine time f_i was calculated using $f_i = (w_i/2) + \sum_{j=0}^{i-1} w_j$.

III. Setup

A. TDC Setup

For each FPGA, we evaluated two hit transitions (i.e., 0-to-1 and 1-to-0), two homogeneous (SSSS and CCCC) sampling patterns, as well as the optimal and various other heterogeneous sampling patterns. Hereafter, we use the notation {hit transition, sampling pattern} to refer to the TDC setup, e.g., {0-to-1, SCSC}.

The TDC module has two operation modes: evaluation mode, in which all TDC channels share one external trigger, and measurement mode, in which each TDC channel has its own trigger input. The purpose of evaluation mode is to

assess the TDC characteristics with minimizing the signal and clock jitters, details of which are discussed in Section IV-C. In the evaluation mode, we determined the optimal heterogeneous sampling TDC setups and compared the nonlinearity values, bin-width distributions, and the root-mean-square (rms) quantization errors between homogeneous and heterogeneous sampling TDCs. On the other hand, in the measurement mode, each TDC channel calculates the arrival time of the hit signal asserted into its own input. This mode was used to measure the time interval between hit signals, which were fed into a TDC pair. We compared the measurement uncertainty values of the time intervals (i.e., single-shot precision) obtained using the homogeneous and heterogeneous sampling TDCs.

B. Experimental Setup

We evaluated both homogeneous and heterogeneous sampling TDCs using two Kintex-7, two Virtex-6, and one Spartan-6. For each of the TDCs implemented in Kintex-7 and Virtex-6, two different chips with 32 different carry chain locations (i.e., 64 in total) were assessed. In the case of Spartan-6, a single chip with 24 different locations was tested. For each implementation, 16, 16, and 6 TDC channels were implemented for Kintex-7, Virtex-6, and Spartan-6, respectively. In addition, homogeneous and heterogeneous sampling TDCs were constrained at the same locations to perform paired t-tests.

The experimental setup that generates random hit signals and time intervals fed into the TDC channels is as follows [40]. The random irradiations from the ^{22}Na point source are converted into FPGA-capable digital hit signals using a scintillation detector [45] and auxiliary electronics. In evaluation mode, this digital hit signal was asserted into the FPGA, and then split within the FPGA. These split hits were shared with all TDC channels. In addition, we fixed the ambient temperature at 25 °C using a temperature-controlled box. In measurement mode to evaluate the measurement uncertainty, a fan-in/fan-out module (N625, CAEN) and a dual delay unit (N108A, CAEN) were added to generate two copies of digital hit signals with a known time interval [40]. The time intervals were generated by a delay unit and ranged from 0 to 10 ns in steps of 0.5 ns. Hit signals with time intervals were then asserted into a TDC pair. The same time intervals were also measured using an oscilloscope (DSO9064A, Agilent). We did not fix the ambient temperature when measuring time intervals in Section IV-E. In addition, we obtained the measurement uncertainty values under various ambient temperatures between 10 °C and 50 °C to verify that the TDC worked under a wide temperature range.

IV. Results and Discussion

For Sections IV-A–IV-D, the TDC operating mode was an evaluation mode to assess TDC characteristics while minimizing signal and clock jitters. We evaluated two homogeneous sampling patterns as well as the optimal and other heterogeneous ones, determined in Section IV-A, with two hit transitions of 0-to-1 and 1-to-0. For measurements in Sections IV-E and IV-F, the TDC operating mode was measurement mode, and the time intervals were measured using a TDC pair. TDC setups that yielded the lowest rms quantization errors in Section IV-C were employed.

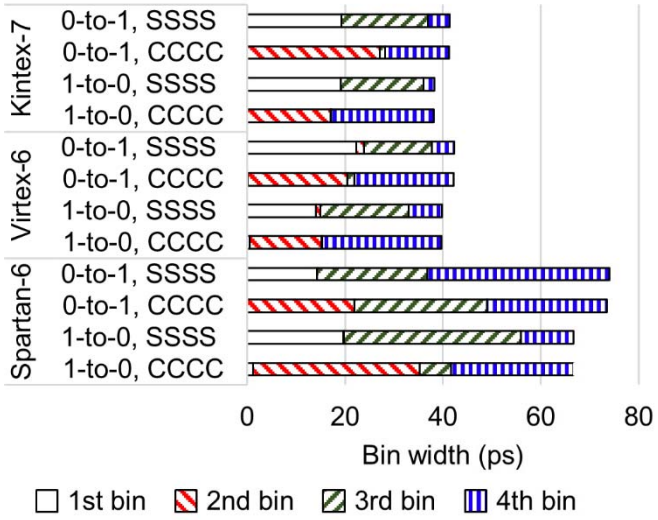

Fig. 4. Average bin widths of the carry element for the homogeneous sampling TDCs.

A. Optimal Heterogeneous Sampling TDC Setup

The procedure determining the optimal heterogeneous sampling TDC setup is conducted in three steps.

The first step is identifying bin widths of S and C bins. The homogeneous sampling TDCs using the sampling patterns of SSSS and CCCC with the hit transition of 0-to-1 are implemented separately, and then respective bin widths are measured using the code density test. The number of samples for each code density test was 102 400, and the ambient temperature was 25 °C.

The second step is tuning bin widths by replacing the carry element outputs corresponding to missing bins, bin widths of which under one-tenth of total propagation time of a carry element, with the other type. This sampling pattern using a hit transition of 0-to-1 is determined as the candidate for the optimal heterogeneous sampling TDC setup. In addition, because the delay pattern is affected by hit transition either 0-to-1 or 1-to-0, the first and second steps are conducted for the other hit transition of 1-to-0, and then, the other candidate using a hit transition of 1-to-0 is determined. As shown in Fig. 4, the second and fourth S bins and the first and third C bins were missing for Kintex-7 and Virtex-6, and thus, the sampling pattern of SCSC was determined as the candidate. The second S bin and first C bin were missing for Spartan-6, and thus, the sampling patterns of SCSS and SCCC were determined as the candidates. These sampling patterns determined using a single carry element can be used in other carry locations, because the delay pattern of a carry element is consistent throughout the FPGA.

The third step is determining the optimal heterogeneous sampling TDC setup of {hit transition, sampling pattern} by comparing the equivalent bin widths of TDCs using the selected candidates in the previous step. The calculation of

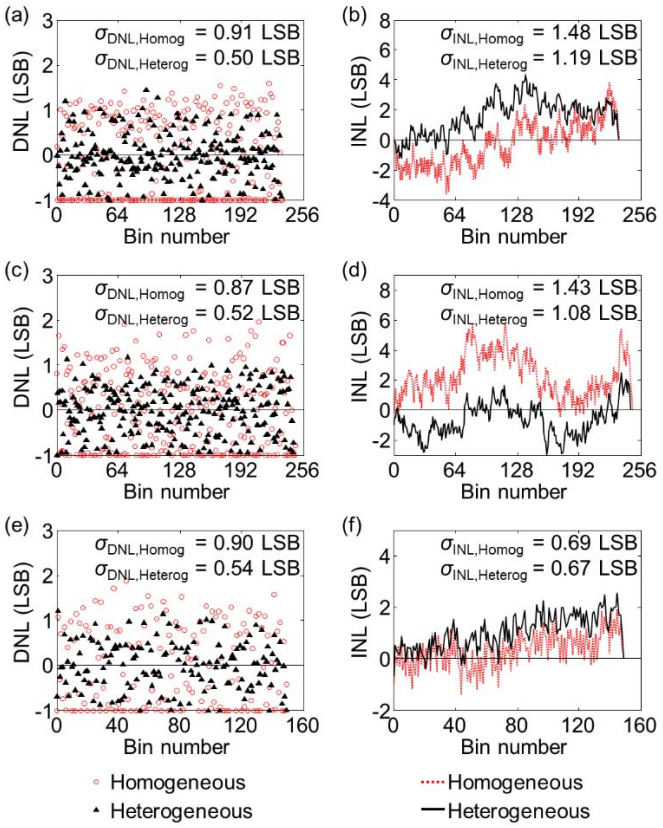

Fig. 5. DNL and INL values using the homogeneous and heterogeneous sampling TDCs. (a) DNL values of Kintex-7. (b) INL values of Kintex-7. (c) DNL values of Virtex-6. (d) INL values of Virtex-6. (e) DNL values of Spartan-6. (f) INL values of Spartan-6. Standard deviation values of the DNL and INL values are noted.

equivalent bin width is described in Section IV-C. The determined optimal heterogeneous sampling TDC setups were as follows: {0-to-1, SCSC} for Kintex-7, {1-to-0, SCSC} for Virtex-6, and {1-to-0, SCSS} for Spartan-6.

B. Nonlinearity and Bin-Width Distribution

To show that the heterogeneous sampling TDC provides better linearity, we compared the differential nonlinearity (DNL) and integral nonlinearity (INL) values of homogeneous and heterogeneous sampling TDCs. We collected 102 400 samples for each measurement to perform a code density test. The DNL and INL values were derived as follows [23]:

$$\mathrm{DNL}_i = \frac{w_i - T_{\mathrm{LSB}}}{T_{\mathrm{LSB}}} \tag{2}$$

$$\mathrm{INL}_i = \sum_{k=0}^{i} \mathrm{DNL}_k. \tag{3}$$

In (2) and (3), w_i is the ith bin width and T_{LSB} is the size of the LSB, which is equal to the average bin width.

Fig. 5 shows the DNL and INL values of a single TDC channel using homogeneous and heterogeneous sampling TDCs. The results using homogeneous and heterogeneous TDC setups that yielded the lowest DNL variations are shown except for those of Spartan-6. Instead, the result using the homogeneous sampling pattern with the hit transition of 1-to-0 is shown to compare the DNL and INL values with similar T_{LSB}. Note that T_{LSB}, 18.4 and 16.7 ps for the hit transitions of 0-to-1 and 1-to-0, respectively, were greatly affected by the hit transition. We used the following setups for the respective TDCs: for Kintex-7, {0-to-1, SSSS} and {0-to-1, SCSC}; for Virtex-6, {1-to-0, SSSS} and {1-to-0, SCSC}; and for Spartan-6, {1-to-0, CCCC} and {1-to-0, SCSS}. The optimal heterogeneous sampling TDC setups determined in Section IV-A yielded the lowest DNL variations.

As shown in Fig. 5(a), (c), and (e), the DNL values improved significantly when adopting heterogeneous sampling; the standard deviation values of the DNL values reduced from 0.91, 0.87, and 0.90 to 0.50, 0.52, and 0.54 LSB for Kintex-7, Virtex-6, and Spartan-6, respectively. More DNL values were close to zero. The DNL values also decreased from [−1, 1.59], [−1, 1.96], and [−1, 1.87] to [−1, 1.45], [−1, 1.18], and [−1, 1.22] LSB, respectively, while the T_{LSB} values were 10.6, 10.1, and 16.7 ps, respectively. In addition, the alternate positive and negative DNL values, which arose when using homogeneous sampling TDCs in Kintex-7 and Virtex-6, were mitigated. The numbers of missing bins corresponding to the −1 LSB were also reduced for all FPGAs.

However, the INL values were not significantly enhanced, as shown in Fig. 5(b), (d), and (f). The standard deviation values of the INL values improved slightly from 1.48, 1.43, and 0.69 to 1.19, 1.08, and 0.67 LSB, respectively. The INL values also decreased from [−3.58, 3.90], [−0.50, 6.80], and [−1.42, 1.90] to [−1.23, 4.30], [−3.03, 2.46], and [−0.70, 2.54] LSB, respectively. Although the INL values were not notably improved, the INL values can be calibrated using the code density test [23], [46].

Improved DNL yielded more uniform bin widths. Fig. 6 shows the normalized bin-width distribution. The results of 64, 64, and 24 TDC channels in the lowest-DNL-variation setups for both homogeneous and heterogeneous sampling TDCs are shown for Kintex-7, Virtex-6, and Spartan-6, respectively. The same setups used to evaluate the nonlinearity values were employed except for the homogeneous sampling TDC setup for Spartan-6; the result using the homogeneous TDC setup of {0-to-1, CCCC} is shown. The values of T_{LSB} were almost the same except for Spartan-6, that is, approximately 10 ps for Kintex-7 and Virtex-6. For Spartan-6, the values of T_{LSB} were 18.4 and 16.7 ps for homogeneous and heterogeneous sampling TDCs, respectively, due to the hit transition difference. The bin widths of heterogeneous sampling TDCs were more uniform than those of homogeneous ones; the standard deviation values of the bin widths were reduced from 9.45, 8.84, and 13.62 to 5.83, 5.83, and 10.80 ps for Kintex-7, Virtex-6, and Spartan-6, respectively. The numbers of missing bins and wide bins were also reduced significantly for all the FPGAs.

C. RMS Quantization Error

TDC involves a quantization process, and the quantization error directly affects the measurement uncertainty. To show that the heterogeneous sampling TDCs reduce the quantization error, we evaluated the calculated rms quantization errors σ_{cal}

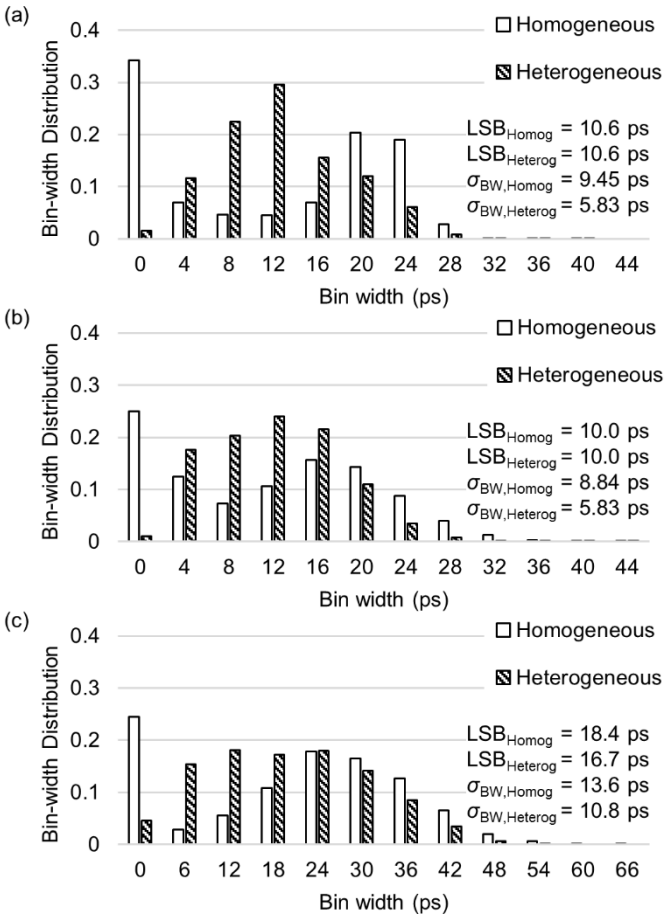

Fig. 6. Normalized bin-width distributions using the homogeneous and heterogeneous sampling TDCs. (a) Kintex-7. (b) Virtex-6. (c) Spartan-6. The T_{LSB} and the standard deviation values of bin widths are noted.

and measured rms quantization errors σ_{meas} of a single channel for homogeneous and heterogeneous sampling TDCs. The same samples used in the code density test were utilized.

The rms quantization error in the case where all bin widths are the same is $T_{\mathrm{LSB}}/\sqrt{12}$ [44]. However, because the bin widths of FPGA-TDCs are nonuniform, σ_{cal} considering the bin-width variation was derived as follows [28], [29], [41], [42]:

$$\sigma_{\mathrm{cal}} = \sqrt{\sum_{i=0}^{M} \frac{w_i^2}{12} \times \frac{w_i}{T_0}} = \frac{w_{\mathrm{eq}}}{\sqrt{12}}. \tag{4}$$

In (4), w_i, M, T_0, and w_{eq} denote the ith bin width, last bin number of the delay line, clock period, and equivalent bin width [28], [29], [41], [42], respectively. The $w_i^2/12$ represents the squared quantization error of the ith bin, and w_i/T_0 indicates the probability density function.

The values of σ_{meas} were obtained from the time interval measurements. Each TDC channel measures the hit arrival time, while the time interval Δt between hit signals measured using a pair of the ith and jth TDC channels is calculated as follows [23]:

$$\Delta t = t_{A,i} - t_{A,j} = (N_{\mathrm{coarse},i} \times T_0 - f_i) - (N_{\mathrm{coarse},j} \times T_0 - f_j). \tag{5}$$

In (5), $t_{A,i}$ and $t_{A,j}$ are the arrival times measured using the ith and jth TDC channels, $N_{\mathrm{coarse},i}$ and $N_{\mathrm{coarse},j}$ are the coarse counts of the ith and jth TDC channels, and f_i and f_j are the fine times of the ith and jth TDC channels, respectively. We fitted a Gaussian function to the time interval measurement and obtained the measurement uncertainty $\sigma_{\mathrm{TI},i,j}$ using the standard deviation value of the Gaussian fit. The $\sigma_{\mathrm{TI},i,j}$ acquired using the coarse-fine TDL TDCs for randomly fed hit signals is the root sum square of the rms quantization errors of the ith and jth TDC channels $\sigma_{\mathrm{meas},i}$ and $\sigma_{\mathrm{meas},j}$, the standard deviation values of the INL values of the ith and jth TDC channels $\sigma_{\mathrm{INL},i}$ and $\sigma_{\mathrm{INL},j}$, the rms reference clock jitter σ_{clk}, the rms jitter within the TDC due to the thermal and supply noise σ_{tdc}, and the ith and jth rms hit signal jitters $\sigma_{\mathrm{sig},i}$ and $\sigma_{\mathrm{sig},j}$ in (6) [42], [46]. All terms in the right-hand side of (6) were assumed to be uncorrelated under the assumption that the hit signals were random.

$$\sigma_{\mathrm{TI},i,j} = \sqrt{\sigma_{\mathrm{meas},i}^2+\sigma_{\mathrm{meas},j}^2+\sigma_{\mathrm{INL},i}^2+\sigma_{\mathrm{INL},j}^2+\sigma_{\mathrm{clk}}^2+\sigma_{\mathrm{tdc}}^2+\sigma_{\mathrm{sig},i}^2+\sigma_{\mathrm{sig},j}^2} \tag{6}$$

where $\sigma_{\mathrm{INL},i}$ and $\sigma_{\mathrm{INL},j}$ can be eliminated when the TDC channels are calibrated using the code density test [46]. In addition, in the evaluation mode, σ_{sig} and σ_{clk} can be minimized in (6) using a shared trigger, because this hit signal was split within the FPGA and fed into every TDC channel with most time delays between the split hits being less than one clock period. In addition, σ_{tdc} was not significant, because the core voltage and the ambient temperature were well regulated by the power module and temperature-controlled box. Thus, $\sigma_{\mathrm{TI},i,j}$ obtained using the shared trigger can be approximated to the root sum square of $\sigma_{\mathrm{meas},i}$ and $\sigma_{\mathrm{meas},j}$ and expressed as a matrix vector multiplication. We obtained σ_{meas} by obtaining the least squares solution as in

$$\begin{pmatrix} \sigma_{\mathrm{meas},0}^2 \\ \sigma_{\mathrm{meas},1}^2 \\ \vdots \\ \sigma_{\mathrm{meas},i}^2 \\ \vdots \\ \sigma_{\mathrm{meas},j}^2 \\ \vdots \\ \sigma_{\mathrm{meas},L-1}^2 \end{pmatrix} = \begin{pmatrix} 1 & 1 & 0 & 0 & \cdots & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & \cdots & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & \cdots & 0 & 1 & 1 \end{pmatrix}^{-1} \times \begin{pmatrix} \sigma_{\mathrm{TI},0,1}^2 \\ \sigma_{\mathrm{TI},0,2}^2 \\ \vdots \\ \sigma_{\mathrm{TI,i,j}}^2 \\ \vdots \\ \sigma_{\mathrm{TI},L-2,L-1}^2 \end{pmatrix}. \tag{7}$$

In (7), L is the number of implemented TDC channels for each implementation: 16, 16, and 6 for Kintex-7, Virtex-6, and Spartan-6, respectively.

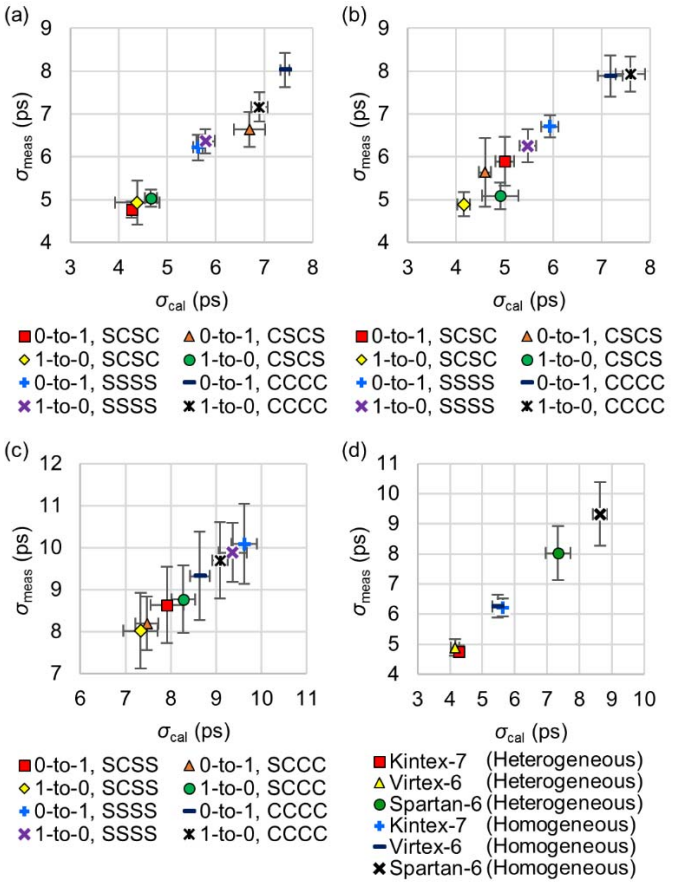

Fig. 7. Calculated rms quantization error σ_{cal} and measured rms quantization error σ_{meas} for different TDC setups. (a) Kintex-7. (b) Virtex-6. (c) Spartan-6. (d) σ_{cal} and σ_{meas} values using the homogeneous and heterogeneous TDC setups that yielded the lowest σ_{cal} and σ_{meas} for each device.

Fig. 7 shows σ_{cal} and σ_{meas} for different TDC setups. The rms quantization error values, which were 3.06, 2.92, and 4.82 ps calculated using $T_{\text{LSB}}/\sqrt{12}$ for Kintex-7, Virtex-6, and Spartan-6, respectively, did not reflect σ_{meas}. In contrast, σ_{meas}, which directly affect σ_{TI}, were well estimated using σ_{cal} and thus using equivalent bin widths [28], [29], [41], [42]. The slight biases between σ_{cal} and σ_{meas} may be introduced by σ_{sig}, σ_{tdc}, and σ_{clk}.

We also performed paired t-tests on σ_{cal} and σ_{meas} and considered the one homogeneous sampling TDC setup that yielded the lowest σ_{cal} and σ_{meas} as the control. The degrees of freedom were 63, 63, and 23 for Kintex-7, Virtex-6, and Spartan-6, respectively. The results are shown in Table I and Fig. 7. The error bars in Fig. 7 indicate the standard deviation values of σ_{cal} and σ_{meas} for 64, 64, and 24 different carry locations. Both σ_{cal} and σ_{meas} improved significantly ($p < 0.05$) using the optimal and other heterogeneous sampling TDCs except for the TDC setup of {0-to-1, CSCS} implemented in Kintex-7. The details are discussed in Section IV-D. In addition, the optimal heterogeneous sampling TDCs provided the lowest σ_{meas} for all the FPGAs. Thus, these optimal heterogeneous sampling TDCs were used for the time interval measurement in Sections IV-E and IV-F. Furthermore, the results were consistent for different carry chain locations, even on different chips. Note that we tested two Kintex-7 and Virtex-6 devices, respectively.

TABLE I
CALCULATED AND MEASURED rms QUANTIZATION ERRORS

Board	Hit transition	Sampling pattern	σ_{cal} (ps)	σ_{meas} (ps)
Kintex-7	0-to-1	SSSS †	5.63 ± 0.10	6.22 ± 0.30
	0-to-1	CCCC	7.42 ± 0.09	8.03 ± 0.40
	1-to-0	SSSS	5.79 ± 0.19	6.37 ± 0.28
	1-to-0	CCCC	6.90 ± 0.18	7.16 ± 0.35
	0-to-1	SCSC	*4.27 ± 0.10	*4.76 ± 0.19
	0-to-1	CSCS	6.69 ± 0.32	6.64 ± 0.41
	1-to-0	SCSC	*4.38 ± 0.45	*4.93 ± 0.51
	1-to-0	CSCS	*4.66 ± 0.12	*5.03 ± 0.20
Virtex-6	0-to-1	SSSS	5.93 ± 0.18	6.71 ± 0.26
	0-to-1	CCCC	7.18 ± 0.25	7.89 ± 0.48
	1-to-0	SSSS †	5.47 ± 0.17	6.26 ± 0.38
	1-to-0	CCCC	7.59 ± 0.30	7.93 ± 0.41
	0-to-1	SCSC	*5.00 ± 0.18	*5.89 ± 0.58
	0-to-1	CSCS	*4.60 ± 0.12	*5.64 ± 0.80
	1-to-0	SCSC	*4.16 ± 0.13	*4.89 ± 0.28
	1-to-0	CSCS	*4.91 ± 0.38	*5.09 ± 0.31
Spartan-6	0-to-1	SSSS	9.62 ± 0.28	10.10 ± 0.95
	0-to-1	CCCC †	8.63 ± 0.22	9.32 ± 1.05
	1-to-0	SSSS	9.36 ± 0.31	9.88 ± 0.70
	1-to-0	CCCC	9.08 ± 0.17	9.70 ± 0.91
	0-to-1	SCSS	*7.91 ± 0.36	*8.64 ± 0.90
	0-to-1	SCCC	*7.47 ± 0.26	*8.19 ± 0.64
	1-to-0	SCSS	*7.33 ± 0.38	*8.02 ± 0.90
	1-to-0	SCCC	*8.28 ± 0.26	*8.77 ± 0.80

The dagger (†) and asterisk (*) indicate the control and statistical significance at a significance level of 0.05, respectively. One-tailed paired t-tests were conducted. Null hypotheses were $\sigma_{\text{cal,Heterog}} \geq \sigma_{\text{cal,Homog}}$ and $\sigma_{\text{meas,Heterog}} \geq \sigma_{\text{meas,Homog}}$. Alternative ones were $\sigma_{\text{cal,Heterog}} < \sigma_{\text{cal,Homog}}$ and $\sigma_{\text{meas,Heterog}} < \sigma_{\text{meas,Homog}}$.

The mean and standard deviation values of σ_{cal} and σ_{meas} for 64, 64, and 24 different carry locations are noted.

D. TDC Transfer Function and Code Density Histogram

In Section IV-C, only one heterogeneous sampling TDC setup of {0-to-1, CSCS} implemented in Kintex-7 aggravated the rms quantization error. This is discussed in conjunction with the transfer function and code density histogram.

The transfer function and the code density histogram of the heterogeneous sampling TDC indicate time quantization by two different types of carry element outputs. Figs. 8 and 9 show the transfer functions and code density histograms of two different heterogeneous sampling TDCs implemented in Kintex-7, respectively. All setups and carry chain location were identical except for the TDC setup; one was the optimal TDC setup of {0-to-1, SCSC} and the other was {0-to-1, CSCS}. The former provided the lowest rms quantization error, while the latter yielded the worst rms quantization error of all the heterogeneous sampling TDCs implemented in Kintex-7.

The degree of overlap between the transfer functions of the S subfine code S_{sub} and C subfine code C_{sub} and the corresponding subfine code difference reflect the bin-width uniformity of the heterogeneous sampling TDC, while the subfine code difference was calculated as follows: for sampling patterns of SCSC and CSCS, $C_{\text{sub}} - S_{\text{sub}}$; for that of SCSS, $3 \times C_{\text{sub}} - S_{\text{sub}}$; and for that of SCCC, $C_{\text{sub}} - 3 \times S_{\text{sub}}$. Theo-

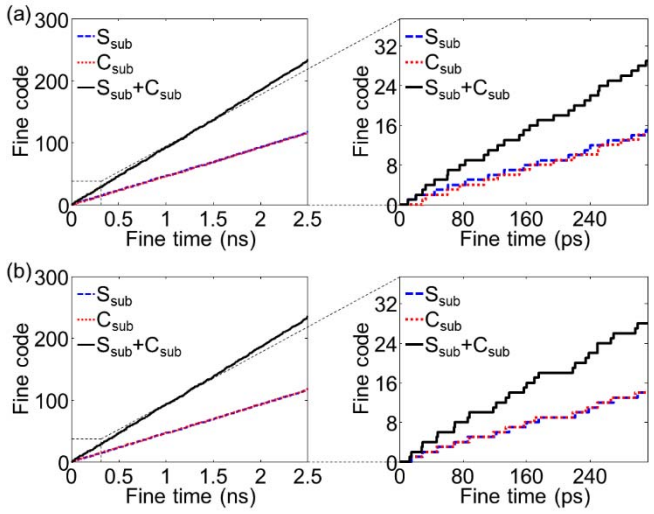

Fig. 8. Transfer functions of the heterogeneous sampling TDCs implemented in Kintex-7. (a) Full and detailed views in the case of the optimal TDC setup of {0-to-1, SCSC}. (b) Full and detailed views in the case of TDC setup of {0-to-1, CSCS}.

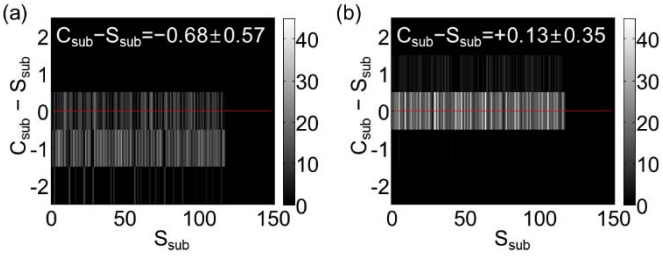

Fig. 9. Code density histograms of the heterogeneous sampling TDCs implemented in Kintex-7. (a) Optimal TDC setup of {0-to-1, SCSC}. (b) TDC setup of {0-to-1, CSCS}. Each element represents its bin width. The mean and standard deviation values of the subfine code differences between the S and C bins are noted.

retically, the mean value of the subfine code differences close to a half-integer corresponds to the case, where the S and C bins subdivide other bins approximately in half in the transfer function, as shown in Figs. 8(a) and 9(a), and thus, yield fine and uniform bin widths. In the case of the mean value close to an integer except for zero, they could subdivide each other, because the S and C bins were not perfectly uniform, and overlapping bins were loosely correlated. However, in the case where the mean value was close to zero, the TDC yielded several wide bins because the highly correlated S and C bins with almost identical bin widths overlapped, as shown in Figs. 8(b) and 9(b). Although highly overlapping transfer functions result in wide bins and higher rms quantization error, the overlap problem can be solved because they can be moved away from each other simply by changing the sampling pattern (e.g., from CSCS to SCSC).

The subfine code differences and their standard deviation values are shown in Table II. The subfine code differences were affected by the TDC setup, and not the carry chain location. In addition, the subfine code differences and their standard deviation values were consistent even for other chips of the same type. This means that the transfer functions and degrees of overlap were also consistent regardless of the carry chain location.

TABLE II
SUBFINE CODE DIFFERENCES BETWEEN S AND C BINS

Board	Hit transition	Sampling pattern	Mean (bin)	Standard deviation (bin)
Kintex-7	0-to-1	SCSC	−0.72 ± 0.05	0.56 ± 0.01
	0-to-1	CSCS	0.05 ± 0.09	0.33 ± 0.03
	1-to-0	SCSC	1.17 ± 0.17	0.56 ± 0.06
	1-to-0	CSCS	2.02 ± 0.12	0.70 ± 0.03
Virtex-6	0-to-1	SCSC	0.98 ± 0.04	0.58 ± 0.02
	0-to-1	CSCS	1.78 ± 0.04	0.67 ± 0.04
	1-to-0	SCSC	−1.33 ± 0.06	0.67 ± 0.03
	1-to-0	CSCS	−0.43 ± 0.05	0.53 ± 0.02
Spartan-6	0-to-1	SCSS	0.13 ± 0.09	1.07 ± 0.03
	0-to-1	SCCC	2.48 ± 0.10	1.00 ± 0.02
	1-to-0	SCSS	−2.08 ± 0.10	1.10 ± 0.03
	1-to-0	SCCC	−0.34 ± 0.08	0.94 ± 0.04

In 'Mean' column, the mean and standard deviation values of the mean values of the subfine code differences for 64, 64, and 24 different carry chain locations are noted. In 'Standard deviation' column, the mean and standard deviation values of the standard deviation values of the subfine code differences are noted.

E. Time Interval Measurement

The main purpose of the TDC is to measure the time interval between physical events with good precision. To verify that the heterogeneous sampling TDCs improve the measurement precision of the time interval owing to reduced quantization error, we evaluated σ_{TI}. The TDC operation mode was changed to measurement mode. The TDC setups that yielded the lowest rms quantization error values were used for both homogeneous and heterogeneous sampling TDCs. Note that the optimal heterogeneous sampling TDC setups provided the lowest rms quantization errors. These setups were as follows: for Kintex-7, {0-to-1, SSSS} and {0-to-1, SCSC}; for Virtex-6, {1-to-0, SSSS} and {1-to-0, SCSC}; and for Spartan-6, {0-to-1, CCCC} and {1-to-0, SCSS}. The time intervals between hit signals from 0 to 10 ns were measured using a TDC pair and an oscilloscope. Pairs of homogeneous and heterogeneous sampling TDCs were tested at the same locations. We collected 51 200 samples for each measurement, and did not fix the ambient temperature to resemble real measurement conditions.

Fig. 10 shows the time intervals measured by the TDCs using homogeneous and heterogeneous sampling TDCs implemented in Kintex-7. The absolute differences between the mean values of time intervals measured by TDCs and oscilloscope were less than 10 ps. In addition, we applied a Gaussian function to the time histogram and acquired σ_{TI} using the standard deviation of the Gaussian fit. Using heterogeneous sampling TDCs, the maximum values of σ_{TI} were reduced from 11.31, 11.27, and 15.57 ps to 8.13, 9.82, and 12.75 ps for Kintex-7, Virtex-6, and Spartan-6, respectively, as shown in Fig. 11. The heterogeneous sampling TDC improved the measurement precision for all the FPGAs.

The slight increases in σ_{TI} with an increase in the time interval were probably due to σ_{clk} [47] and σ_{sig}, degraded by the long delay cable of the delay unit. The values of σ_{sig} of time intervals measured using the oscilloscope were

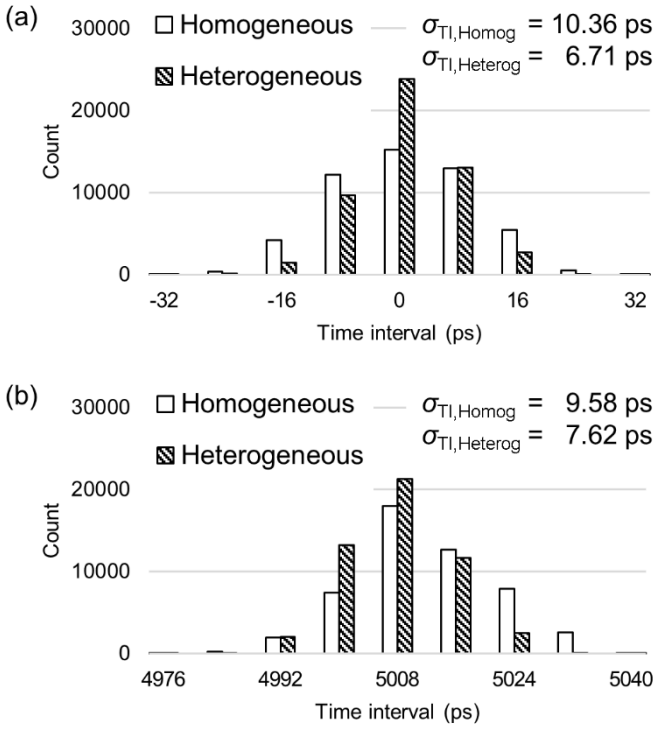

Fig. 10. Time histograms measured using the homogeneous and heterogeneous sampling TDCs implemented in Kintex-7. (a) Time interval within one clock period (i.e., the time interval of 0 ns). (b) Time interval greater than one clock period (i.e., the time interval of 5 ns). The values of σ_{TI} are noted.

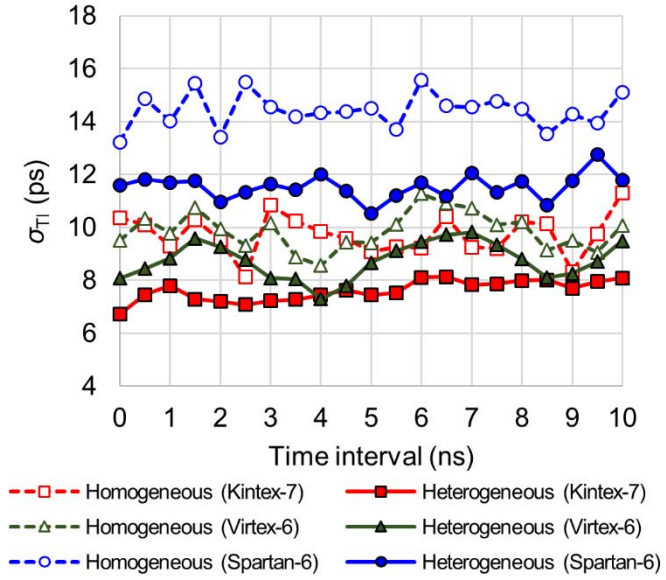

Fig. 11. σ_{TI} for the time intervals.

from 1 to 3 ps. However, σ_{sig} were not subtracted from σ_{TI}, because σ_{sig} contributing to σ_{TI} were negligible and measurement uncertainty of oscilloscope were involved.

F. Robustness to Temperature Disturbance

In a real experimental environment, voltage and temperature disturbances can deteriorate TDC performance [29], [35], [38], [40]. Although the core voltage was regulated by the power module, it was also affected by the ambient temperature [40]. To verify that the heterogeneous sampling TDCs provide good precision for a wide temperature range, the time interval fixed at zero was measured under temperatures ranging from 10 °C to 50 °C in steps of 10 °C. Using the same TDC setups employed to evaluate σ_{TI} in Section IV-E, we collected 102 400 samples for each measurement. The fine codes were calibrated using the calibration LUT generated at the respective temperature for both homogeneous and heterogeneous sampling TDCs [29], [40], [44].

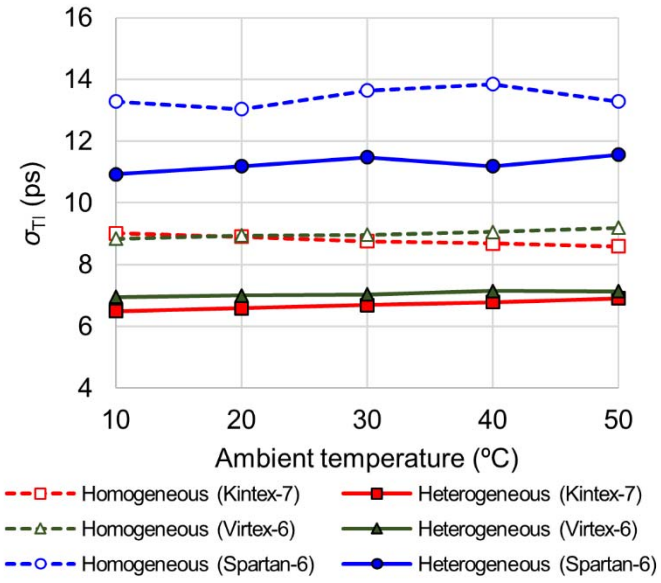

Fig. 12. σ_{TI} for the ambient temperatures from 10 °C to 50 °C.

TABLE III
RESOURCE USAGE FOR A SINGLE TDC CHANNEL

Board	Sampling pattern	Resource usage	
		Flip-flops	LUTs
Kintex-7 (KC705)	Homogeneous	1626 (0.40%)	570 (0.28%)
	Heterogeneous	1641 (0.40%)	577 (0.28%)
Virtex-6 (ML605)	Homogeneous	1626 (0.54%)	570 (0.38%)
	Heterogeneous	1641 (0.54%)	577 (0.38%)
Spartan-6 (SP605)	Homogeneous	861 (1.58%)	300 (1.10%)
	Heterogeneous	787 (1.44%)	261 (0.96%)

The numbers of flip-flops and LUTs used. The percentage of resource utilization is given in parentheses. The total numbers of available slices are 50950, 37680, and 6822 for the KC705, ML605, and SP605, respectively. In each slice, eight flip-flops and four LUTs are available.

The T_{LSB} increased as the ambient temperature rose [40]. However, the values of σ_{TI} were almost consistent regardless of the ambient temperature, as shown in Fig. 12. The values of σ_{TI} were less than 9.02, 9.19, and 13.85 ps for the homogeneous sampling TDCs implemented in Kintex-7, Virtex-6, and Spartan-6, respectively, while those for the heterogeneous ones were less than 6.91, 7.15, and 11.56 ps, respectively. For a wide temperature range, the heterogeneous sampling TDCs yielded lower σ_{TI} than the homogeneous ones.

G. Conversion Rate and Resource Usage

All TDC modules were pipelined at the 400-MHz reference CLK. The dead time, defined as the time after each

TABLE IV
TDC COMPARISON TABLE

Ref	Method	Chip, Process (nm)	TDC Characteristics					Resource usage	
			T_{LSB} (ps)	σ_{TI} (ps)	DNL (LSB)	INL (LSB)	Dead time (ns)	Flip-flops	LUTs
[37]	TDL	Kintex-7, 28	22.7	36.4 [f]	2.6	3.4	30	N/S	N/S
[38]	TDL	Virtex-6, 40	10	19.6	[–1, 1.5]	[–2.25, 1.61]	3.3	N/S	N/S
[40]	TDL	Virtex-6, 40	10	12.83	[–1, 1.91]	[–2.20, 3.93]	N/S	N/S	N/S
[39]	TDL	Spartan-6, 45	25.5	17.7 [f]	5	N/S	N/S	N/S	N/S
[27]	TDL [a]	Virtex-5, 65	30	15	[–1, 3]	[–4, 4]	30 [e]	571 [j]	1,064 [j]
[28]	MDL [b]	Virtex-6, 40	2.93	7.6	[–0.7, 0.8] [g]	[–1, 0.7] [g]	18.75 [e]	N/S	N/S
	MDL [c]	Virtex-6, 40	1.47	5.9	N/S	N/S	18.75 [e]	N/S	N/S
[29]	MDL [c]	Spartan-6, 45	1.14	6	N/S	–19.36	N/S	N/S	N/S
[30]	CYC [d]	Virtex-4, 90	12	10	[–1, 1.1]	[–9, 8]	50	2,081 [j]	3,280 [j]
[31]	CYC	Spartan-3, 90	42	56	–0.98	–4.17	N/S	N/S	N/S
[32]	CYC	SmartFusion, 130	63.3	61.7	[–0.55, 0.28]	[–0.72, 0.63]	1,410 [e]	N/S	N/S
[33]	VM	Spartan-3, 90	75	300 [f]	[–1, 2.5] [h]	[–2.5, 3.0] [h]	0	N/S	N/S
[34]	WUA	Cyclone II, 90	30	25	N/S	N/S	5	1,621 [i, j]	1,621 [i, j]
	WUB	Cyclone II, 90	N/S	10	N/S	N/S	45	6,851 [i, k]	6,851 [i, k]
[35]	WUA	Virtex-4, 90	50 [e]	9	N/S	N/S	N/S	N/S	N/S
[36]	WUA	LatticeECP2/M, 90	10	10.3	[–0.96, 2.74]	N/S	30	N/S	20,000 [l]
[48]	DLL	Commercial chip	13	8	N/S	N/S	5	N/S	N/S
[49]	N/S	Commercial chip	3.8	20	N/S	N/S	N/S	N/S	N/S
[50]	DLL +RC	Instrument ASIC, 250	25	35	3	2.5 [g]	5	N/S	N/S
[51]	N/S	Instrument	27	66	[–1, 1]	N/S	190	N/S	N/S
[52]	SINE	Instrument	5	N/S	N/S	N/S	10	N/S	N/S
This work	TDL	Kintex-7, 28	10.6	8.13	[–1, 1.45]	[–1.23, 4.30]	5	1,641 [j]	577 [j]
		Virtex-6, 40	10.1	9.82	[–1, 1.18]	[–3.03, 2.46]	5	1,641 [j]	577 [j]
		Spartan-6, 45	16.7	12.75	[–1, 1.22]	[–0.70, 2.54]	5	787 [j]	261 [j]

TDL = single tapped-delay line, MDL = multi-delay line, CYC = cyclic or multi-time measurement, VM = Vernier matrix, WUA = wave-union A (finite step response), WUB = wave-union B (infinite step response), DLL = delay-locked loop, DLL+RC = DLL+RC delay line, SINE = sine-wave interpolation, N/S = not specified. The LSB was equal to T_{LSB}. Measurement uncertainty σ_{TI} was obtained using the maximum value of the standard deviation values of the time interval measurements [23]. Nonlinearity was evaluated using [minimum value, maximum value] or a single parameter representing the worst-case value. DNL = differential nonlinearity before calibration, INL = integral nonlinearity before calibration. Dead time is the time after each measurement before the TDC is able to perform the next measurement. Resource usage represents the numbers of utilized flip-flops and LUTs. Note that the total numbers of available flip-flops and LUTs can differ each other according to chips. [a]bin decimation by two, [b]eight delay lines, [c]16 delay lines, [d]sampling during four clocks, [e]maximum value, [f]mean value, [g]nonlinearity value after calibration, [h]inferred from the figure, [i]number of logic elements consisting of a four-input LUT and a flip-flop, [j]resource usage for a single channel, [k]resource usage for eight channels, [l]resource usage for 16 channels.

measurement before the TDC is able to perform the next measurement, was two clock periods (i.e., 5 ns): one clock period for processing time and one clock period for recovery time of the delay line. Thus, the expected maximum conversion rates were the same at 200 MS/s for both homogeneous and heterogeneous sampling TDCs.

The resource usage was almost the same, as shown in Table III. The numbers of carry elements used as the delay line were the same for both homogeneous and heterogeneous sampling TDCs. The small differences were introduced by the encoder, and not the delay line, as mentioned in Section II-C.

H. Comparison With Other TDCs

In Table IV, the characteristics and the resource usage of the heterogeneous sampling TDC are compared with those of our previous work [40], the most recent FPGA-TDCs, and high-end commercial TDCs. Our previous work [40], which employed two TDLs covering the different halves of the clock period to minimize clock skew problem introduced by the clock distribution network and the fast on-the-fly INL calibrator, was based on homogeneous sampling TDC, and thus, bin widths cannot be tuned. In contrast, a heterogeneous sampling TDC can tune bin widths, and thus, DNL values and σ_{TI} were enhanced compared with other TDL TDCs [37]–[40]. In addition, σ_{TI} obtained using a simple TDL TDC were comparable with those acquired using other complex TDC architectures. Moreover, unlike other TDC architectures, the heterogeneous sampling TDC improved precision while retaining the strengths of the TDL TDC, that is, short dead time and multichannel capacity. The proposed TDC with high-throughput capacity would be useful when the TDC measures arrival times of hit signals fed from multiple trigger inputs [39]. Compared with the high-end commercial chips [48], [49] and instruments [50]–[52], the proposed FPGA-TDC has comparable performance and advantage of design flexibility.

V. Conclusion

In this paper, we proposed a novel TDC architecture of a heterogeneous sampling TDC that is able to tune the bin width, and thus, the nonlinearity, rms quantization error, and measurement uncertainty were reduced compared with those of the ordinary TDL TDC for three types of FPGAs. Single-shot precision under 10 ps was achieved for Kintex-7 and Virtex-6. The improved linearity, particularly for the DNL value, can enhance the performance of not only the TDL TDC, but also other FPGA carry chain-based TDC designs.

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