Highly Integrated FPGA-Only Signal Digitization Method Using Single-Ended Memory Interface Input Receivers for Time-of-Flight PET Detectors

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***Abstract*—We propose a new highly integrated field-programmable gate array (FPGA) only signal digitization method for individual signal digitization of time-of-flight positron emission tomography (TOF PET). We configured I/O port of the FPGA with a single-ended memory interface (SeMI) input receiver. The SeMI is a single-ended voltage-referenced interface that has a common reference voltage per I/O Bank, such that each SeMI input receiver can serve as a voltage comparator. The FPGA-only digitizer that uses the single-ended input receivers does not require a separate digitizing integrated chip, and can obtain twice as many signals as that using LVDS input receivers. We implemented a highly integrated digitizer consisting of 82 energy and 82 timing channels using a 28-nm FPGA. The energy and arrival time were measured using a 625-ps binary counter, and a 10-ps time-to-digital converter (TDC), respectively. We first measured the intrinsic characteristics of the proposed FPGA-only digitizer. The SeMI input receiver functioned as the voltage comparator without undesirable offset voltage. The standard deviation value of the time difference measured using two SeMI input receivers with respective TDCs was less than 14.6 ps RMS. In addition, we fed signals from the TOF PET detectors to the SeMI input receivers directly and collected data. The TOF PET detector consisted of a $3 \times 3 \times 20$ mm^3 LYSO crystal coupled with a silicon photomultiplier. The energy resolutions were 7.7% and 7.1% for two TOF PET detectors. The coincidence resolving time was 204 ps full width at half maximum. The SeMI digitizer with a high-performance signal digitizer, processor, and high-speed transceivers provides a compact all-in-one data acquisition system.**

***Index Terms*—FPGA-only digitizer, individual signal readout, single-ended interface, time-of-flight (TOF), time-of-flight positron emission tomography (TOF PET).**

I. Introduction

POSITRON emission tomography (PET) is a functional imaging tool that detects pairs of back-to-back gamma rays and provides a 3D distribution of radioactive tracers labeled with the positron emitters. Compared with the conventional PET, time-of-flight (TOF) PET can localize the position of the tracer within the line of response by measuring arrival time difference precisely [1]–[6]. The TOF PET provides higher image quality for better lesion detection. In addition, TOF PET is robust to discrepancies in attenuation correction map that are common in multimodal imaging systems such as PET/CT and PET/MRI [2], [7].

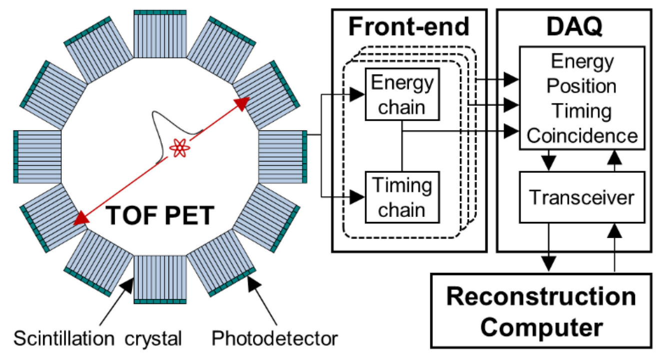

Fig. 1. Time-of-flight positron emission tomography (TOF PET).

To maximize TOF performance, PET detectors, front-end electronics, and data acquisition systems should have fast timing responses as shown in Fig. 1. A silicon photomultiplier (SiPM) is a state-of-the-art photosensor that converts light photons into fast electrical signals; however, it has high granularity and large terminal capacitance. Multiplexing granulated SiPMs to handle a large number of SiPMs increases total detector capacitance and degrades TOF performance.

Individual signal readout from each SiPM draws the best timing performance [8], [9]. In addition, individual signal readout improves spatial resolution by identifying and recovering inter-crystal scattering events accurately [10]. However, a large number of signal digitization channels are required to read individual signals from the granulated SiPMs.

One of the integrated signal digitization methods involves using application specific integrated circuits (ASICs) [4], [5], [11]–[13]. The ASICs can digitize signals with high performance, low power consumption, and small footprint. However, given that most ASICs use a low-voltage differential signaling (LVDS) interface for communication, an additional

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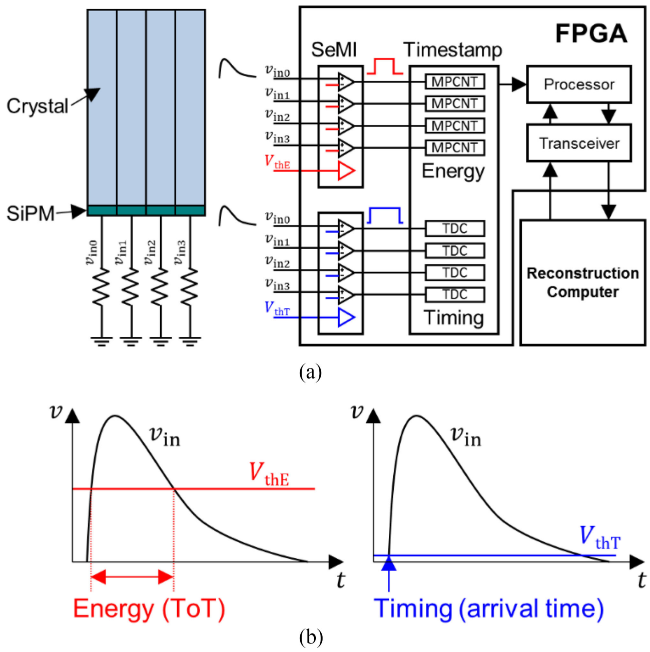


Fig. 2. Conceptual diagram of the SeMI digitizer. (a) Individual signal readout of SiPM-based TOF PET detector. (b) Energy and timing measurement methods using the SeMI digitizer.

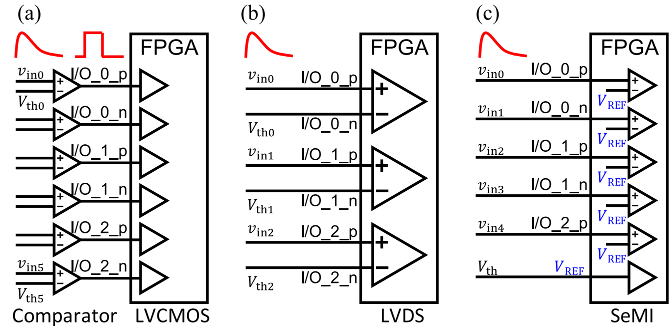


Fig. 3. Time-based signal digitization methods. (a) Conventional signal digitization method using the discrete voltage comparators. (b) FPGA-only signal digitization method using the LVDS input receivers. (c) Proposed FPGA-only signal digitization method using the single-ended memory interface (SeMI) input receivers.

field-programmable gate array (FPGA) is required to process data and transfer data packets to a computer.

Another integrated signal digitization method involves using an FPGA-only digitizer that uses an LVDS input receiver as a voltage comparator to digitize signals [14]–[17]. The FPGA-only digitizer has the advantage that the FPGA itself digitizes the signal, processes the data, and communicates with the computer. However, each LVDS input receiver requires a pair of configurable FPGA input/output (I/O) ports. Therefore, this method has the drawback that the number of signal digitization channels is less than half the total number of available I/O ports.

In this paper, we propose a new highly integrated FPGA-only signal digitization method using single-ended voltage-referenced input receivers instead of LVDS input receivers. The voltage comparator implemented using the single-ended interface of the FPGA has the advantage that almost all FPGA configurable I/O ports can be used as signal digitization channels, because each single-ended interface requires only a single configurable I/O port.

II. Single-Ended Memory Interface (SeMI) Digitizer

We refer to a new FPGA-only digitizer as a single-ended memory interface (SeMI) digitizer where the analog signal is digitized by the single-ended voltage-referenced input receiver and the logic state is read by timestamp modules implemented in the same FPGA as shown in Fig. 2.

A. SeMI Input Receiver

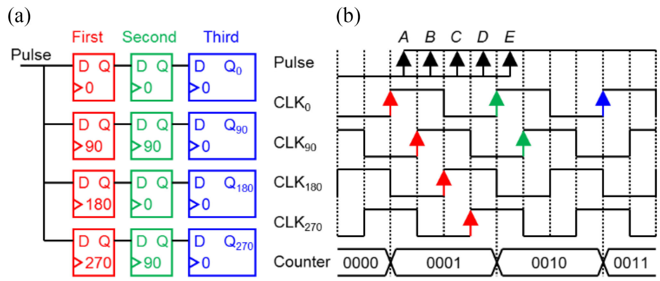
Most FPGA I/O ports have configurable I/O buffers that support a variety of single-ended / differential and supply-voltage-ratioed / voltage-referenced I/O standards. We configured the I/O buffers with single-ended voltage-referenced input receivers such as high-speed transceiver logic (HSTL) and stub-series terminated logic (SSTL) receivers that are widely used in memory interfaces. We refer to the single-ended memory interface as SeMI hereinafter.

The principle of using the SeMI input receiver as the voltage comparator is as follows. The logic state of the SeMI input receiver is determined by comparing the input signal to the adjustable common reference voltage V_{REF}. If the input signal is greater than V_{REF}, the logic state of the receiver is 1. Otherwise, the logic state is 0. The V_{REF} is shared with multiple SeMI input receivers in the I/O Bank that indicates a group of I/Os. In a typical application, the V_{REF} is designed to be half the supply voltage of the I/O Bank, but can be adjusted by the user. Therefore, by applying analog signals and the common threshold to the SeMI input receivers and a dedicated V_{REF} receiver, respectively, the SeMI input receivers function as multiple voltage comparators sharing the common threshold V_{REF}.

A notable advantage of the SeMI input receiver is that each requires only one configurable I/O port as shown in Fig. 3. The conventional time-based digitization methods use the discrete comparators and FPGA input receivers [18]–[22]. The LVDS input receiver requires two FPGA I/O ports: one for the analog signal and the other for the threshold [14]–[17]. Therefore, the proposed method can digitize the analog signals without discrete comparators and handle twice as many signals as the LVDS input receivers. For example, for the 7-series FPGA of Xilinx, each I/O Bank contains 50 I/O ports that can be configured into 50 single-ended or 24 differential interfaces. The I/O Bank shares a common V_{REF} and two I/O ports in a Bank are dedicated ports where the V_{REF} from -0.5 to 2.0 V can be applied externally. Therefore, 48 SeMI input receivers in a Bank can be used as comparators. In addition, a typical FPGA has four or more Banks with hundreds of configurable I/O ports. Thus, it can digitize hundreds of signals directly using the SeMI input receivers.

B. Multiphase Counter (MPCNT)

A binary counter with phase detecting flip-flops operating in four different clock phases was used to measure the energy of the gamma rays interacting with PET detectors [14]. We refer to this as the multiphase counter (MPCNT) hereinafter.



(c)

	A	B	C	D	E
Counter output	0010	0010	0010	0010	0011
Q_0	0	0	0	0	0
Q_{90}	1	0	0	0	1
Q_{180}	1	1	0	0	1
Q_{270}	1	1	1	0	1
Phase code	00	01	10	11	00
MPCNT code	001000	001001	001010	001011	001100

Fig. 4. Multiphase counter (MPCNT). (a) Schematic of MPCNT. (b) Timing diagram of MPCNT. *A*, *B*, *C*, *D*, and *E* represent logic transitions at respective time. (c) Truth table for logic transitions of *A*, *B*, *C*, *D*, and *E*.

The operation principle of MPCNT is as follows. As shown in Fig. 4, the MPCNT consisted of a 12-bit binary counter operating at a clock period of 2500 ps with a phase 0°, and the phase detecting flip-flops operating at the same clock period with phases of 0°, 90°, 180°, and 270°. These clock signals CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} were generated by an on-chip phase-locked loop (PLL). The first-layer flip-flops sampled the logic state of the SeMI input receiver at the rising edge of each clock signal. The logic states sampled at the rising edges of CLK_0 and CLK_{180} were fed into the second-layer flip-flops operating at CLK_0. Those sampled at the rising edges of CLK_{90} and CLK_{270} were fed into the second-layer flip-flops operating at CLK_{90}. The logic states were in-phased by the third-layer flip-flops operating at CLK_0. The in-phased states were encoded into a two-bit phase code using the look-up table and concatenated with the 12-bit output of the binary counter operating at CLK_0. In the consequence, this MPCNT provided a 14-bit binary count with a time resolution of $2500/4 = 625$ ps and the dynamic range of $2^{14} \times 625$ ps $= 10.240$ μs. In addition, the MPCNT was fully pipelined and the FPGA resource usage was negligible.

Energy information was measured using a time-over-threshold (ToT) method. We measured the ToT value by directly inputting detector output signal into the SeMI input receiver and using the MPCNT to measure time difference between the rising and falling edges of the digitized signal. The ToT value was then converted into the energy value using the ToT calibration curve. Hereinafter, we call this method as the SeMI ToT.

C. Time-to-Digital Converter (TDC)

The TDC was used to measure the arrival time of the gamma rays interacting with PET detectors. A tapped-delay-line TDC consisted of a 12-bit coarse counter and a fine time interpolator as shown in Fig. 5 [23]–[25]. The 12-bit coarse counter operated at the clock period of 2500 ps. The fine time interpolator consisted of a 256-tap carry chain with a bin-width tuning method (i.e., heterogeneous sampling of sums (S) and carry-outs (C)) [24], sampling flip-flops, a hit detect flag, a fine-code encoder, and a fine-time calibrator. The resolution was 10.7 ps.

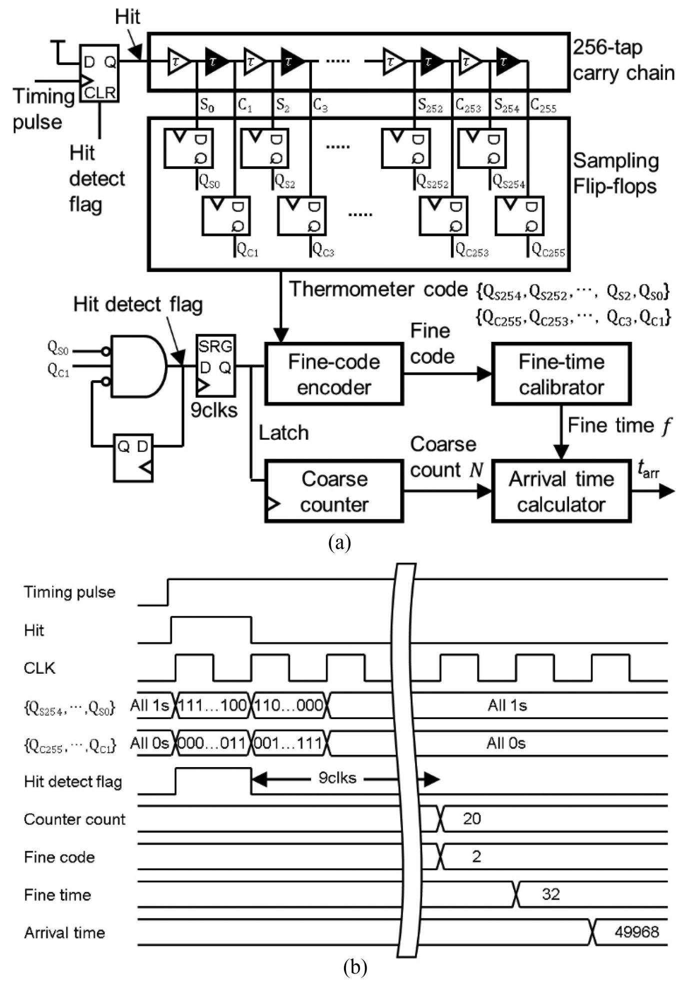


Fig. 5. Tapped-delay-line time-to-digital converter (TDC) implemented using a carry chain of the FPGA. (a) Schematic of TDC. (b) Timing diagram of TDC.

The asynchronous trigger was delayed with changing the states of delay elements, and sampled by flip-flops at the rising time of the main clock signal. The hit detect flag was asserted when the hit signal propagated the first two delay elements (S_0 and C_1) [25]. In addition, hit detect flag was asserted for a single clock cycle using the sequential feedback loop. The 9-clock-cycle delayed hit detect flag using a shift register (SRG) was used to latch both coarse count N and fine code. The sampled states (also known as thermometer code) were converted into a fine code using a fine-code encoder [25]. The fine code was calibrated to a fine time f of which the dynamic range was 0 to 2500 ps using a fine-time calibrator. The arrival time t_{arr} was calculated as follows (1):

$$t_{\mathrm{arr}} = N \times 2500\,\mathrm{ps} - f \tag{1}$$

The TDC was fully pipelined and can measure the arrival time of the next timing pulse after 5 ns from the time when the previous timing pulse was asserted [24]. For low-cost FPGAs with a small number of FPGA resources, FPGA resources for TDC can be reduced by partially sampling the taps of the delay line by compromising TDC resolution. In addition, the TDC

TABLE I
NUMBER OF IMPLEMENTED CHANNELS IN A KINTEX-7 EVALUATION KIT

I/O Bank	Number of accessible I/O ports	Number of accessible V_{REF} ports	Number of implemented digitization channels
12	38	2	36 timing channels
13	36	1	28 energy channels
15	2	0	0
16	36	1	28 energy channels
17	36	1	26 energy channels
18	48	2	46 timing channels

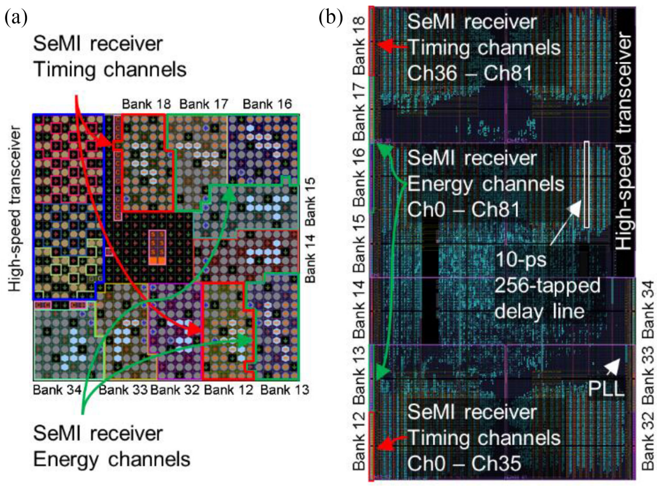


Fig. 6. Layout of the SeMI digitizer using a Kintex-7 FPGA. (a) I/O ports. 164 I/O ports were configured with SeMI input receivers. (b) Implementation.

can be shared by multiple SeMI input receivers [26], when the scintillation pulse width is short. The timing pulses of TOF detectors are typically short, because the fast scintillation crystals have short decay times [8], [9], [27], [28] and the timing signals of SiPM are usually high-pass filtered [29], [30].

D. Implementation of the SeMI Digitizer

We implemented the SeMI digitizer in a Kintex-7 evaluation kit (KC705, Xilinx). The Kintex-7 evaluation kit has 196 accessible ports in six I/O Banks (Bank 12, 13, 15, 16, 17 and 18) through the FPGA mezzanine card (FMC) connectors and the on-board SMA connectors as shown in Table I.

We first characterized the intrinsic performance of SeMI input receivers by configuring the I/O buffers of multiple I/O Banks with HSTL and SSTL input receivers.

We then implemented a highly integrated digitizer consisting of 82 energy and 82 timing channels using 171 I/O ports (164 ports for digitization channels and 7 ports for V_{REF}) in five I/O Banks as shown in Table I and Fig. 6. The SeMI input receivers were configured with SSTL input receivers. For the 164-channel implementation, 38% of the registers, 51% of the LUTs, and 70% of the slices were utilized.

The input signal was directly fed into the SeMI input receiver and terminated to the ground using a 50 Ω resistor. A bypass capacitor of 0.1 μF was placed between V_{REF} and the ground. The V_{REF} values were adjusted using a 12-bit DAC (LTC2625, Linear Technology) from 0 to 2.048 V in steps of 0.5 mV.

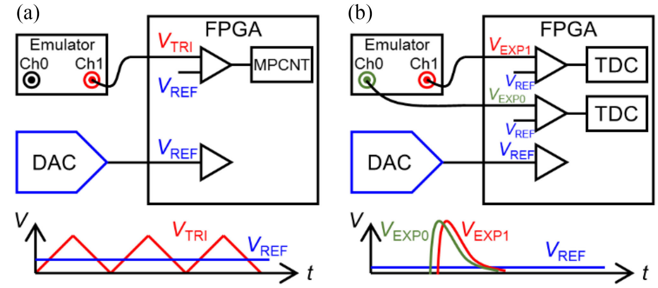


Fig. 7. Experimental setup for intrinsic performance characterization of the SeMI digitizer. (a) ToT measurement. (b) Arrival time difference measurement.

III. EXPERIMENTAL SETUP FOR INTRINSIC PERFORMANCE CHARACTERIZATION OF THE SEMI DIGITIZER

A. Time-Over-Threshold (ToT)

We measured the ToT values for the test pulse to verify that the SeMI input receiver functioned as a voltage comparator and the MPCNT correctly measured the pulse width. As shown in Fig. 7(a), we used the detector emulator (DT5800D, CAEN) to apply the triangular pulses V_{TRI} to five SeMI input receivers located in different I/O Banks (Banks 12, 13, 16, 17, and 18). The period, offset voltage, and peak-to-peak voltage of the V_{TRI} were 1 μs, 1 V, and 2 V, respectively. In addition, we changed the V_{REF} from 0.05 V to 1.95 V in steps of 0.05 V. We measured each pulse width when the V_{TRI} was higher than V_{REF}. We obtained 51,200 pulse widths for each measurement. The mean and full width at half maximum (FWHM) values of the measured pulse widths were evaluated.

B. Timing

We measured the arrival time difference and evaluated the time uncertainty of the SeMI digitizer to verify that the SeMI input receiver provided a fast and precise logic transition and the TDC measured the arrival time with fine time resolution.

We used the detector emulator to generate two copies of V_{EXP0} and V_{EXP1} with a fixed arrival time difference from -3008.4 to $+3008.4$ ps in steps of 501.4 ps as shown in Fig. 7(b). The 10–90% rise, decay times, peak amplitude were 7 ns, 40 ns, and 1 V, respectively. The V_{EXP0} and V_{EXP1} were applied to two SeMI input receivers located at the I/O Bank 12. The V_{REF} of 50 mV was applied. In addition, we measured the fixed time difference for 10-90% rise times of 7 (minimum value) and 21 ns, V_{REF} of 5, 10, 20, and 50 mV, and various slew rates. We calculated the slew rate by the slope of the line connecting the 10% and 90% of the maximum amplitude.

The arrival time difference was measured using two TDCs. We obtained 51,200 events for each time difference, and fitted time difference histogram into a Gaussian function. The mean and standard deviation (SD) values were measured.

IV. EXPERIMENTAL SETUP FOR INDIVIDUAL SIGNAL READOUT OF TOF PET DETECTORS

After characterizing the intrinsic performance of the SeMI digitizer, we collected data from the TOF PET detectors with

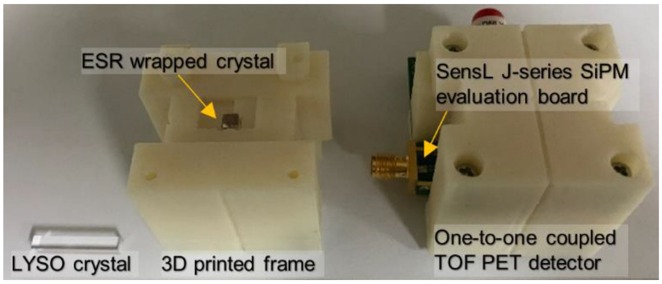


Fig. 8. One-to-one coupled TOF PET detector.

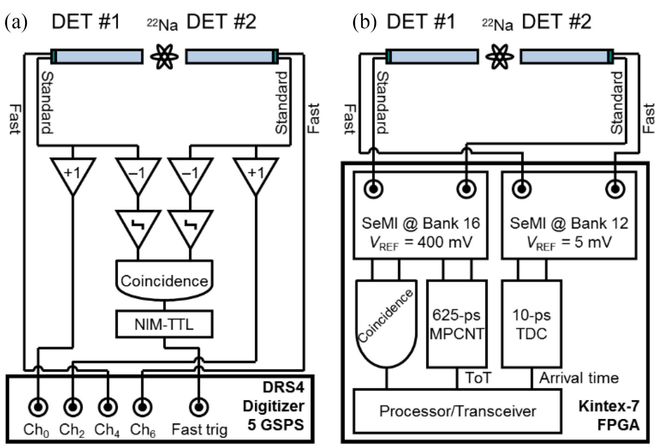


Fig. 9. Experimental setup for performance evaluation of TOF PET detectors using (a) waveform digitizer and (b) SeMI digitizer.

one-to-one coupling and individual signal readout. In addition, we used a high-performance waveform digitizer (DT5742B, CAEN) to collect reference data from the same detectors.

A. TOF PET Detector

We assembled two identical one-to-one coupled detectors, each with a $3 \times 3 \times 20$ mm^3 LYSO crystal (EPIC Crystal) and a SensL J-series SiPM evaluation board (MicroFJ-SMA-30035, SensL) as shown in Fig. 8. The crystal was wrapped with the enhanced specular reflectors (ESR, 3M) except for the exit face, and coupled with the SiPM using the optical grease (BC-630, Saint-Gobain). The detector was mechanically fixed and optically isolated using an in-house frame built using the 3D printer (Mojo, Stratasys).

The SensL J-series SiPM has bias input, standard output, and fast output terminals connected to the cathode, anode, and internal capacitors, respectively. The bias voltage of 32.0 V that corresponded to the overvoltage of 7.5 V was applied.

The ^{22}Na point source was located between two detectors and 51,200 coincidence events were collected. The distance between the crystal faces was 1 cm. The ambient temperature was 25 °C and no thermal regulation was applied.

B. Data Acquisition Using the Waveform Digitizer

The in-house fan-out modules and nuclear instrument modules (NIMs) were used to obtain the coincidence events as shown in Fig. 9(a). The standard output terminals of both detectors were fed into a two-channel fan-out module. Each channel provided one non-inverted and one inverted output with the respective voltage gains of $+1$ and -1. The inverted outputs were sequentially fed into the discriminator module (N843, CAEN), the coincidence module (N455, CAEN), and following the NIM-TTL-NIM adapter (N89, CAEN) to generate the coincidence trigger. We obtained data using the waveform digitizer in two experimental setups. In the first setup, we sampled both standard and fast output signals as shown in Fig. 9(a). In the second setup, we detached fast outputs and sampled only standard output signals.

The waveform digitizer sampled the coincidence events at a sampling rate of 5 GSPS and a resolution of 12 bit. To obtain the arrival time, we applied the digital leading edge discrimination method to the fast or standard output signals. The leading edge of the signal was interpolated 20 times, and the threshold voltage for time pickoff was 5 mV.

In addition, we measured energy information from the standard output signal samples using two methods. One was the integration method of summing the standard output signals for 160 ns after baseline correction. The other was *in-silico* ToT method, and we applied a digital threshold voltage of 400 mV to the standard output signal after baseline correction. We obtained the ToT calibration curve from the events within energy window of 250 to 750 keV by fitting *in-silico* ToT values and integrated values into the exponential function. We then converted *in-silico* ToT values into the energy values using the ToT calibration curve.

C. Data Acquisition Using the SeMI Digitizer

Two energy and two timing channels of the 164-channel SeMI digitizer were used to obtain data of TOF PET detectors. Energy channels were the SSTL input receivers in the Bank 16 with a V_{REF} of 400 mV. Timing channels were the SSTL input receivers in the Bank 12 with a V_{REF} of 5 mV.

As with experimental setup using the waveform digitizer, we obtained data in two experimental setups. In the first setup, the standard and fast output terminals were input directly into the I/O ports located at Banks 16 and 12, respectively, as shown in Fig. 9(b). In the second setup, the standard output signals were split and then input into the I/O ports located at Banks 16 and 12.

The ToT value was obtained from the standard output signal using the MPCNT, and then the ToT value was converted to energy information using the calibration curve obtained using the waveform digitizer. The arrival time was measured using the TDC from the fast and standard output signals in the respective experimental setups. In addition, the standard output signals were used to generate a coincidence window within the FPGA [31]. The coincidence events within both coincidence windows were obtained.

D. Data Analysis

The energy peak positions and energy resolutions were evaluated by fitting the photopeak of the energy histogram to the Gaussian function. The coincidence resolving time (CRT) was evaluated by fitting the time difference histogram of coincidence events within both energy windows into the Gaussian function. The energy window was twice the FWHM of the

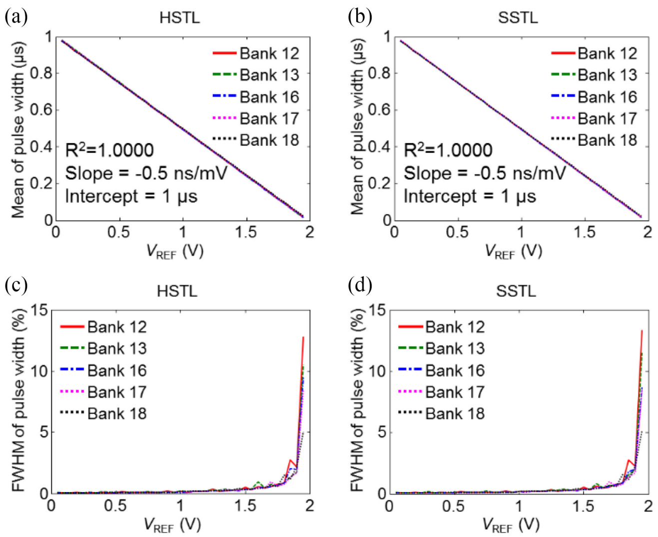


Fig. 10. ToT measurement using the SeMI ToT. Mean and FWHM values of the measured ToT of the triangular pulse V_{TRI} against the reference voltage V_{REF}. The SeMI input receiver was configured as HSTL or SSTL input receiver.

photopeak. The energy resolution and the CRT values were expressed as the FWHM value of the Gaussian function.

V. Experimental Results on the Intrinsic Performance of the SeMI Digitizer

A. Time-Over-Threshold (ToT)

The SeMI inputs in five I/O Banks functioned as the voltage comparators without undesirable offset voltage, and the MPCNT accurately measured the ToT value. As shown in Figs. 10(a) and 10(b), the mean value of ToT was linearly changed with the V_{REF} value. We fitted the ToT and V_{REF} values to a linear function. The R^2 value was 1.0000. The mean values of the slope and intercept were –0.5 ns/mV and 1 μs, respectively, and corresponded to the V_{TRI} and the V_{REF} accurately. This indicates that there was no input offset voltage for the SeMI input receiver and the common threshold. Thus, offset voltage calibration is not required.

In addition, the SeMI input receiver and the MPCNT precisely measured the ToT value. As shown in Figs. 10(c) and 10(d), the maximum FWHM value was less than 3%, except for the very short ToT.

The SeMI input receivers implemented in multiple I/O Banks for ToT measurements showed very similar performance. This represents that all configurable I/O ports in multiple I/O Banks can be used as voltage comparators of equivalent performance. In addition, the HSTL and SSTL I/O configuration did not affect the ToT measurements.

B. Timing

The SeMI input receivers provided a fast and precise transition for the analog signal. The TDCs accurately and precisely measured arrival time differences. Fig. 11(a) show the merged time difference histogram. The applied time differences between V_{EXP0} and V_{EXP1} were accurately measured as shown in Fig. 11(b). In addition, the SD values were less than 14.6 ps RMS (= 34.4 ps FWHM) as shown in Fig. 11(c).

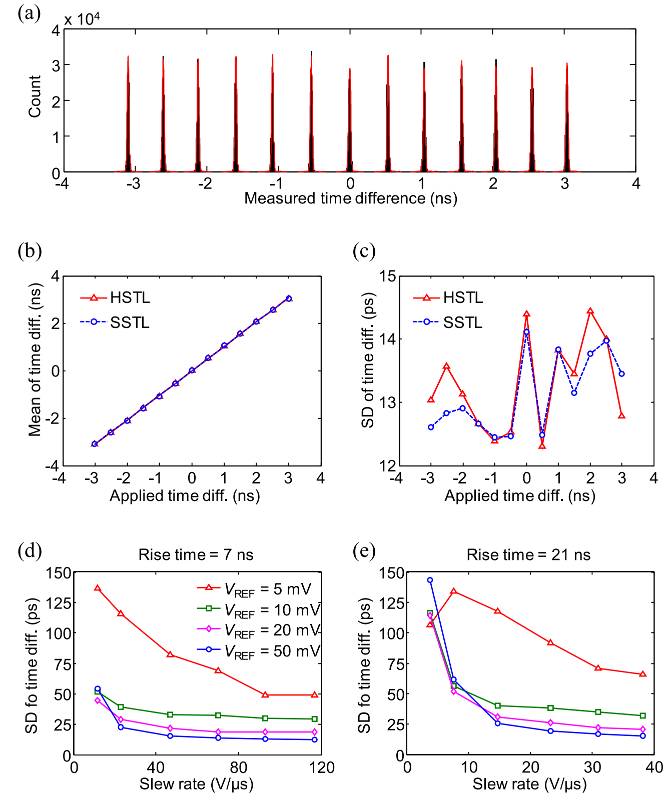


Fig. 11. Arrival time difference measurement. (a) Merged arrival time difference histogram for signals with rise times of 7 ns and V_{REF} of 50 mV. (b) Mean values of the measured time differences. (c) Standard deviation (SD) values of the measured time differences. The SeMI input receivers were configured as HSTL or SSTL input receivers. (d) SD values of the measured time differences for signals with rise times of 7 ns against V_{REF} and slew rate. (e) SD values of the measured time differences for signals with rise times of 21 ns against V_{REF} and slew rate.

In addition, the crosstalk between SeMI input receivers was negligible. Two SeMI input receivers were implemented on the I/O ports that can be used as a pair of differential interfaces. For the time difference of 0 ns, two exponential pulses arrived at the SeMI input receivers almost simultaneously, but the SD value was less than 14.4 ps RMS. This shows that multiple timing chains can be implemented on the same I/O Bank without crosstalk. The HSTL and SSTL I/O configuration did not affect the time difference measurements.

We also evaluated the SD values of the measured time differences against rise times, V_{REF} values, and slew rates as shown in Figs. 11(d) and 11(e). The SD values were degraded as V_{REF} and slew rate decreased as with LVDS input receivers [17]. However, it is difficult to analyze the jitter of SeMI input receiver with respect to V_{REF} and slew rate, because the measured SD values contained the source jitter that can vary against V_{REF} and slew rate.

VI. Experimental Results on Individual Signal Readout of TOF PET Detectors

A. Signal Properties

Table II summarizes the signal properties of two TOF PET detectors for 511 keV event.

TABLE II
SIGNAL PROPERTIES OF TWO TOF PET DETECTORS FOR 511 KEV EVENT

	Det #1		Det #2	
Output terminal	Standard	Fast	Standard	Fast
Peak amplitude (mV)	954	97	808	99
10-90% rise time (ns)	22.1	3.0	21.3	2.8
Slew rate (V/μs)	34.5	29.9	30.3	32.6

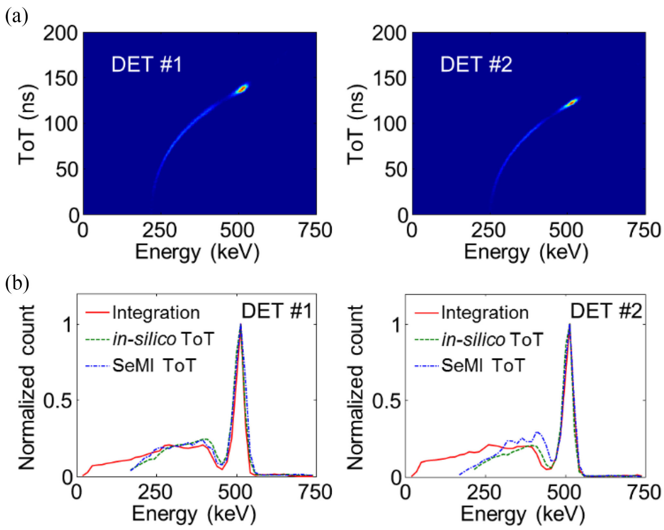


Fig. 12. (a) Relation of energy and ToT. (b) Normalized energy histograms using integration, *in-silico* ToT, and SeMI ToT methods.

B. Energy

Fig. 12(a) shows the relation between energy measurements using integration and *in-silico* ToT methods when using a waveform digitizer. The energy measurement using the integration method was normalized so that the photopeak position was 511 keV. For both detectors, the *in-silico* ToT values versus the integration values were fitted to the exponential curve to obtain the ToT calibration curves.

Fig. 12(b) shows the energy histograms obtained using the integration, *in-silico* ToT, and SeMI ToT methods. The *in-silico* ToT and SeMI ToT values were calibrated using the ToT calibration curves. The energy histogram obtained using the SeMI ToT was similar to that obtained using the integration method for an energy range greater than 350 keV. The photopeak was well resolved using the SeMI ToT. The energy resolutions of two detectors using the integration method were 6.1% and 6.8%. Those using the *in-silico* ToT method were 7.5% and 6.5%. Those using the SeMI ToT were 7.7% and 7.1%. We did not apply SiPM nonlinearity correction for both data obtained using the waveform digitizer and the SeMI digitizer. The SeMI ToT method with fine precision (FWHM <3%) enables one to obtain comparable energy resolution with the 5-GSPS waveform digitizer.

C. Coincidence Resolving Time (CRT)

Fig. 13(a) shows the time difference histograms for the first experimental setup collecting both standard and fast output signals. Fig. 13(b) shows the time difference histograms for the second experimental setup collecting only standard output signals. The energy windows generated by the integration, *in-silico* ToT, and SeMI ToT methods were applied. The CRT values when the arrival times were pickoff using the fast output signals were 203, 205, and 204 ps FWHM, respectively. The CRT values when the arrival times were pickoff using the standard output signals were 231, 228, and 243 ps FWHM, respectively.

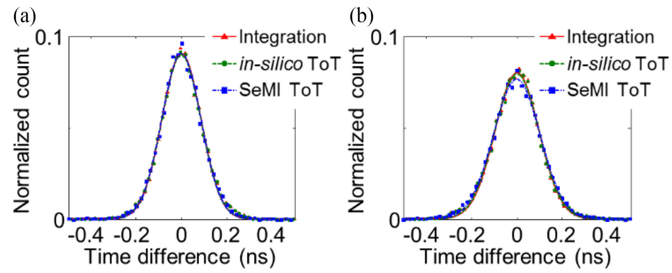


Fig. 13. (a) Normalized time difference histograms when the arrival times were pickoff using the fast output signals. (b) Normalized time difference histograms when the arrival times were pickoff using the standard output signals. The energy windows generated using integration, *in-silico* ToT, and SeMI ToT methods were applied.

When the arrival times were pickoff using the fast output signals, the CRT value obtained using the SeMI digitizer was comparable with those obtained using the waveform digitizer. When the arrival times were pickoff using the standard output signals, the CRT value obtained using the SeMI digitizer was slightly degraded compared with those obtained using the waveform digitizer. The CRT values obtained using the fast output signals were better than those obtained using the standard output signals, because the fast output signal is a high-pass filtered signal with dark current suppressed [30].

The TOF PET with a CRT of 204 ps FWHM is expected to improve the image signal-to-noise ratio by a factor of 3.4 for patients with an effective diameter of 35 cm compared with a non-TOF PET [6]. In clinical practice, better image quality provides higher lesion contrast, shorter scan time, and lower radiation exposure to the patients.

VII. PROSPECTS

The SeMI digitizer is useful for applications that require multichannel signal digitization, because the modern FPGAs have 100 to 1500 configurable I/O ports. Therefore, it is well-suited for PET scanners using the individual signal readout to achieve maximum performance [32], [33] and the total-body PET scanners with a long axial field-of-view to increase the sensitivity of the scanner [34]–[37]. In addition, the SeMI digitizer features compact circuit, requiring no discrete comparator, ADC, or TDC. Therefore, the SeMI digitizer would be useful for simultaneous PET/MRI scanners where early signal digitization is preferred but the volume of the PET scanner restricted [33], [38]–[42].

In addition, the SeMI digitizer can be used for various time-based signal digitization and multiplexing methods. The multi-voltage threshold (MVT) digitizer can be implemented by feeding the signal to multiple SeMI input receivers located in different I/O Banks. The charge-to-time converter (as known as pulse width modulation) that requires the common threshold is well-suitable for the SeMI digitizer [18], [43], [44]. The block detector using a hybrid resistor-capacitor charge division method can be read using ToT method, because the pulse shape does not change with respect to position [45]. Given that the time-based multiplexing method employs a common threshold for time pickoff, the delay grid multiplexing and strip-line multiplexing that use the transit time differences to obtain position information can be read by the SeMI digitizer [46], [47].

Compared with LVDS input receivers, the LVDS input receiver is more flexible than the SeMI input receiver. Each digitization channel using LVDS input receiver has an individual threshold [14–17], and thus thresholds for MVT method can be optimized. In addition, dynamic threshold method and sigma-delta modulation can be applicable [15]. The SeMI input receiver is well-suitable for ToT and charge-to-time converter, because the SeMI input receiver does not have undesirable offset voltage. Furthermore, the SeMI input receiver can pickoff the arrival time from the fast outputs of the SensL SiPMs with a V_{REF} of 5 mV without any front-end electronics and provided a TOF performance of 204 ps FWHM.

The SeMI digitizer has the inherent advantages of FPGA: fast time to market and low non-recurring engineering. Therefore, the SeMI digitizer is expected to be useful not only in PET scanners [48]–[51] but also in a variety of biomedical applications such as *x*-ray CT, ultrasound medical imaging [52], electrical impedance imaging [53], photoacoustic imaging [54], [55] and neural probe [56] that require a fast multichannel signal digitizer.

VIII. Conclusion

We proposed a novel high-density FPGA-only digitizer that integrates signal digitization, processing, and communication. Almost every configurable I/O port can be used as a high-performance voltage comparator. The SeMI input receiver digitized analog signals, and the following MPCNT and TDC measured ToTs and arrival times accurately and precisely. In addition, we demonstrated the feasibility of the SeMI digitizer as a highly integrated DAQ system by individually reading signals from TOF PET detectors. The SeMI digitizer has great prospects as a highly integrated all-in-one DAQ system for biomedical applications.

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