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To cite this article: Jun Yeon Won *et al* 2020 *Phys. Med. Biol.* **65** 155007

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PAPER

Comparator-less PET data acquisition system using single-ended memory interface input receivers of FPGA

RECEIVED
12 September 2019REVISED
16 March 2020ACCEPTED FOR PUBLICATION
3 April 2020PUBLISHED
29 July 2020Jun Yeon Won^{1,2,4,5} , Guen Bae Ko^{2,3,4,5}, Kyeong Yun Kim³, Haewook Park^{1,4}, Seungeun Lee^{1,4}, Jeong-Whan Son³ and Jae Sung Lee^{1,2,3,4} ¹ Department of Nuclear Medicine, Seoul National University College of Medicine, Seoul 03080, Korea² Institute of Radiation Medicine, Medical Research Center, Seoul National University College of Medicine, Seoul 03080, Korea³ Brightonix Imaging Inc., Seoul 04782, Korea⁴ Department of Biomedical Sciences, Seoul National University College of Medicine, Seoul 03080, KoreaE-mail: sonjohn@snu.ac.kr and jaes@snu.ac.kr**Keywords:** charge-to-time converter (QTC), FPGA-based digitizer, data acquisition (DAQ) system, time-based signal digitization, brain PET scanner**Abstract**

In this study, we propose a linear field-programmable gate array (FPGA)-based charge measurement method by combining a charge-to-time converter (QTC) with a single-ended memory interface (SeMI) input receiver. The QTC automatically converts the input charge into a dual-slope pulse, which has a width proportional to the input charge. Dual-slope pulses are directly digitized by the FPGA input/output (I/O) buffers configured with SeMI input receivers. A proof-of-concept comparator-less QTC/SeMI data acquisition (DAQ) system, consisting of 132 energy and 33 timing channels, was developed and applied to a prototype brain-dedicated positron emission tomography (PET) scanner. The PET scanner consisted of 14 sectors, each containing 2×1 block detectors, and each block detector yielded four energy signals and one timing signal. Because a single QTC/SeMI DAQ system can receive signals from up to eight sectors, two QTC/SeMI DAQ systems connected using high-speed gigabit transceivers were used to acquire data from the PET scanner. All crystals in the PET block detectors, consisting of dual-layer stacked lutetium oxyorthosilicate (LSO) scintillation crystal and silicon photomultiplier arrays, were clearly resolved in the flood maps with an excellent energy resolution. The PET images of hot-rod, cylindrical, and two-dimensional Hoffman brain phantoms were also acquired using the prototype PET scanner and two QTC/SeMI DAQ systems.

1. Introduction

In positron emission tomography (PET), we can achieve the high intrinsic spatial resolution of block detectors using a small-sized scintillation crystal array and a light sharing readout. Based on the light sharing readout scheme, we can resolve the pixelated crystals that have a smaller element size than a photosensor array (e.g. array-type silicon photomultiplier and multi-anode photomultiplier tube) coupled with the crystals (Cherry *et al* 1997, Ko *et al* 2016a, Son *et al* 2016b). In addition, the light sharing readout scheme enables depth-of-interaction (DOI) encoding on the flood histogram of PET block detectors with stacked crystal arrays (Liu *et al* 2001, Nan *et al* 2003, Tsuda *et al* 2004, Hong *et al* 2008, Ito *et al* 2010, Lee 2010, 2011, Son *et al* 2016a). The DOI information mitigates parallax errors that degrade the spatial resolution at the peripheral region.

Output electric signals from the photosensor array in block detectors with the light sharing readout scheme are usually multiplexed using analog charge division circuits to reduce the number of output signals (Siegel *et al* 1996, Popov *et al* 2003, Olcott *et al* 2005, Kwon and Lee 2014, Park *et al* 2017). Based on the amount of electric charge measured from the output channels of the multiplexing circuit, we can estimate

⁵ JYW and GKB contributed equally for this work.

the position and energy information regarding the annihilation photon interaction with the scintillation crystal. Therefore, a data acquisition (DAQ) system that measures charge information linearly is required to accurately identify all crystal positions and achieve high spatial resolution. In addition, PET scanners consist of dozens to hundreds of block detectors, requiring DAQ systems consisting of a large number of simplified readout channels.

A conventional circuit used in PET data acquisition (DAQ) systems to digitize the analog signal from the energy channels of a multiplexing circuit is a flash or pipelined analog-to-digital converter (ADC) (Fontaine *et al* 2009, Haselman *et al* 2009, Choong *et al* 2015). The ADC samples the signal waveform and provides the charge information linearly. However, it is difficult to increase the number of energy channels with an ADC because of the large power consumption and the bulky size.

A time-based signal digitization method that uses a timing circuit to obtain both energy and timing information is power- and space-efficient method to simplify DAQ systems and further to increase the number of readout channels for PET scanners. Thus, time-based signal digitization methods have been developed using not only discrete circuits but also application-specific integrated circuits (ASICs).

Time-over-threshold (ToT) method is a straightforward time-based signal digitization method that applies a single threshold to the signal and extracts the energy and timing information from the pulse width and the transition time, respectively (Kipnis *et al* 1997). NINO ASIC using the ToT method contains 8-channel amplifiers and discriminators (Anghinolfi *et al* 2004). ToT has the advantage that it requires only a single voltage comparator for both energy and timing measurements. However, the ToT method has the disadvantages of non-linear energy measurement and poor energy and/or timing resolutions (Grant and Levin 2014). The low threshold to detect the early photons degrades the energy resolution and the high threshold for energy discrimination deteriorates the timing resolution. Thus, the dual-threshold or linearized ToT to apply low and high thresholds for the timing and energy channels, respectively, was developed to obtain good energy and timing resolutions for the time-of-flight (ToF) PET detectors (Njejmama *et al* 2013, Rolo *et al* 2013, Grant and Levin 2014, Harion *et al* 2014). In addition, STiC and TOFPET ASICs using dual-threshold ToT include time-to-digital converters (TDCs) and simplify the back-end electronics.

A dynamic ToT method uses a single voltage comparator with an adaptive threshold to improve energy linearity and resolution. The threshold starts at a low level and increases gradually after the signal crosses the low threshold (Shimazoe *et al* 2012, Yonggang *et al* 2014). This method can achieve both good energy and timing resolution because low and high thresholds are used for timing and energy measurements, respectively. A new dynamic ToT using an adaptively changing saw-tooth shape threshold can reconstruct the signal and discriminate pulse shape for DOI measurement (Ko and Lee 2019). However, the dynamic threshold requires complex discrete circuits to generate threshold.

The multi-voltage threshold (MVT) method uses multiple comparators and obtains multiple samples to reconstruct the analog signals (Kim *et al* 2009, Xie *et al* 2009). The energy and timing information is extracted from the reconstructed signals. However, the MVT method requires multiple comparators for each signal, thus degrading the level of integration.

A charge-to-time converter (QTC) involving an integrator collects the input charge and provides a dual-slope pulse of which width is proportional to the input charge. The gated QTC is widely adapted in ASIC because digitally controlled switches and an associated digital controller can be highly integrated with the integrator (Nishino *et al* 2009, Francesco *et al* 2016). Contrary to the gated QTC, the non-gated QTC uses a diode instead of switch and controller and automatically controls its idle, charge, and discharge phases (Liu *et al* 2010, Parl *et al* 2012). Thus, non-gated QTC with the advantage of simple circuitry has been implemented using discrete circuits.

A 1-bit sigma-delta modulator consists of an integrator, a voltage comparator, and a feedback loop containing a 1-bit digital-to-analog converter (DAC) (Koch *et al* 1986, Rebeschini *et al* 1989). The voltage comparator monitors the integrated difference between the input signal and the DAC output. When the integral difference is greater than the threshold voltage, the voltage comparator is triggered and the DAC output is generated. In consequence, the density of 'ones' at the voltage comparator output is proportional to the input signal.

The ASIC-based readout method is more power- and space-efficient than the discrete circuit-based method because it can include multi-channel amplifiers, voltage comparators, and TDCs in a small package. Contrary to ASIC, the discrete circuit-based method is faster in the design flow and lower in engineering for implementation and testing. In addition, the discrete circuit-based methods can be simplified by adding precise time-measuring capabilities, including voltage comparators and TDCs, to a field-programmable gate array (FPGA) used for processor and data transfer (Sousa *et al* 2004, Wu *et al* 2007, Xi *et al* 2013, Moskal *et al* 2016, Zhao *et al* 2017, 2018).

Previously, we proposed a highly integrated FPGA-only signal digitization method by configuring the FPGA input/output (I/O) buffer with a single-end memory interface (SeMI) input receiver to use each FPGA

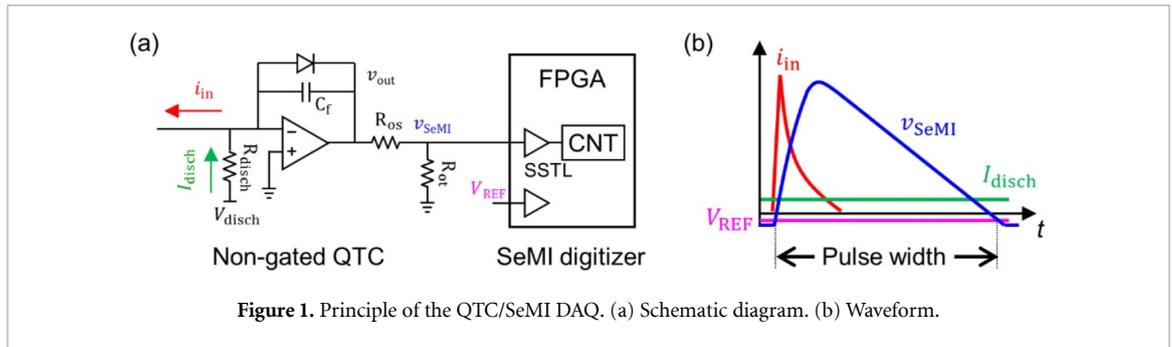


Figure 1. Principle of the QTC/SeMI DAQ. (a) Schematic diagram. (b) Waveform.

I/O port as a high-performance voltage comparator (Won and Lee 2018). The operating principle using each FPGA I/O port as a voltage comparator is as follows. Most FPGAs have hundreds of configurable I/O ports grouped into I/O Banks. I/O ports of the same I/O Bank share the supply and the reference voltages. The FPGA I/O port configured with the SeMI input receiver shares the common reference voltage, and the logic state of the SeMI input receiver is determined by comparing the input signal with the common reference voltage. Thus, the SeMI input receivers of each I/O Bank operate as voltage comparators sharing the common threshold.

We used a plane time-over-threshold (ToT) method to obtain the energy information from the one-to-one coupled PET detectors. However, the ToT method has limitations in collecting data from the light sharing PET detectors because the ToT method intrinsically suffers from energy non-linearity. In addition, most charge division circuits distort the energy signal waveform with respect to the position, making it difficult to obtain the crystal position using the plane ToT method (Park *et al* 2017).

In this study, we propose a new FPGA-based signal digitization method that combines a QTC with a SeMI input receiver to measure the charge information linearly and simplify the DAQ system. Contrary to the ToT method, the QTC converts the input charge into pulse width linearly (Liu *et al* 2010, Parl *et al* 2012, Bieniosek *et al* 2013). Thus, we can use the QTC to obtain data from the high-resolution stacked DOI PET detectors with the light sharing scheme and charge division circuits. In addition, the QTC is well-suited for use with the SeMI digitizer because it requires a common threshold for charge measurements (Won and Lee 2018). Furthermore, we implemented the DAQ systems based on the comparator-less QTC/SeMI technology to collect data from a prototype high-resolution brain PET scanner.

2. Materials and methods

2.1. Principle of the QTC/SeMI DAQ system

The comparator-less QTC comprises a non-gated QTC and a SeMI input receiver. The non-gated QTC comprises an integrator, a diode, and a constant current source. It generates a dual-slope pulse, which has a width proportional to the input charge because the charges of the current difference between the input current (i_{in}) and the constant discharge current (I_{disch}) are stored in the feedback capacitor (C_f) of the integrator (Liu *et al* 2010, Parl *et al* 2012).

The detailed principle of the non-gated QTC is as follows (figure 1). When i_{in} is zero, the QTC is in the idle phase and v_{out} is at the baseline, corresponding to $-V_{fwd}$, where V_{fwd} is the forward voltage drop across the diode. When i_{in} is greater than I_{disch} , the QTC is in the charge (run-up) phase. The diode blocks and $i_{in} - I_{disch}$ charges C_f , after which v_{out} increases. When i_{in} is smaller than I_{disch} , the QTC is in the discharge (run-down) phase, the diode allows the current $I_{disch} - i_{in}$ to flow, and if i_{in} is zero in the discharge phase, v_{out} decreases linearly until v_{out} restores $-V_{fwd}$. The pulse width during the charge and discharge phases is proportional to the input charge by applying a threshold voltage that is slightly greater than the baseline.

The input signal to the SeMI input receiver (v_{SeMI}) is a linearly attenuated signal of v_{out} using voltage dividing resistors (R_{os} and R_{ot}). The upper voltage level of v_{SeMI} is limited to be less than the I/O Bank supply voltage of 2.5 V. The SeMI input receiver is implemented by configuring the FPGA I/O buffer with a stub-series terminated logic (SSTL) input receiver and applying the threshold voltage (V_{REF}) to the dedicated reference voltage port. The pulse width while v_{SeMI} is greater than V_{REF} is measured by a binary counter or a TDC implemented in the same FPGA.

2.2. Implementation of the QTC/SeMI DAQ system

The QTC/SeMI DAQ system implemented in this study comprises a QTC add-on board, a Kintex-7 evaluation kit (KC705, Xilinx), and switched-mode power supplies. It is housed in a 19-inch 3 U aluminum case, as illustrated in figure 2. Each DAQ system includes 132 energy and 33 timing channels.

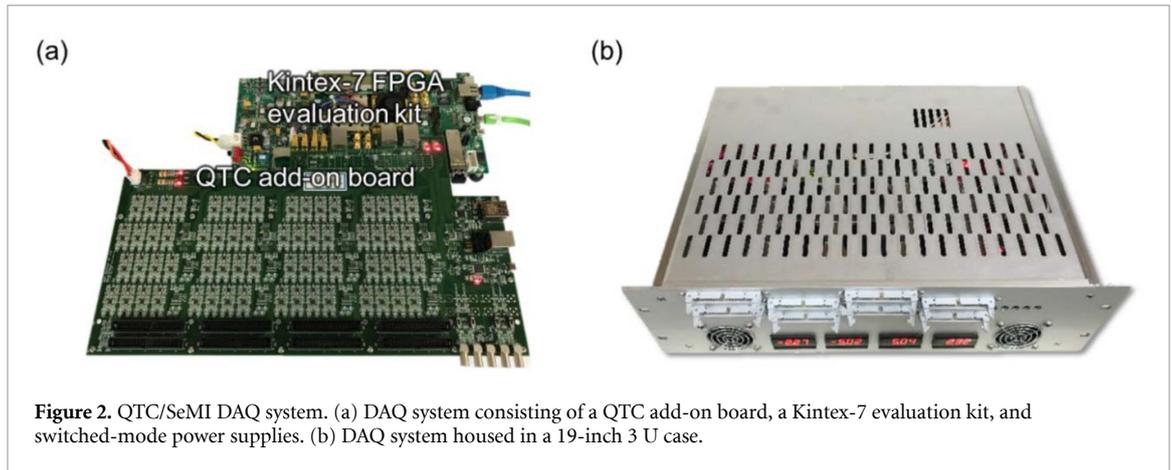


Figure 2. QTC/SeMI DAQ system. (a) DAQ system consisting of a QTC add-on board, a Kintex-7 evaluation kit, and switched-mode power supplies. (b) DAQ system housed in a 19-inch 3 U case.

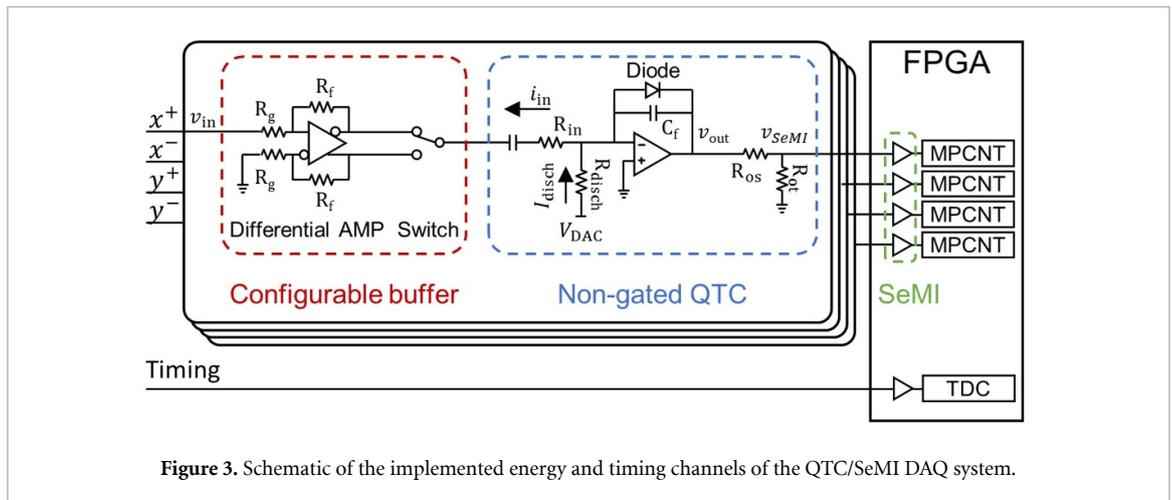


Figure 3. Schematic of the implemented energy and timing channels of the QTC/SeMI DAQ system.

The KC705 has 192 accessible ports in five I/O Banks (Bank 12, 13, 16, 17, and 18) through two FPGA mezzanine card (FMC) connectors. The 132 energy channels were implemented by configuring 132 FPGA I/O buffers in I/O Banks 12, 13, 16, and 17 with the SSTL input receivers. The V_{REF} of -0.1 V was generated using a variable resistor with each end connected to $+5$ V and -5 V, and applied to five semi-dedicated V_{REF} ports. The number of accessible V_{REF} ports for I/O Banks 12, 13, 16, and 17 of the KC705 is two, one, one, and one, respectively. A bypass capacitor of 0.1 μ F was placed between each V_{REF} port and the ground. The 33 timing channels were implemented by configuring 33 FPGA I/O buffers in I/O Bank 18 with low voltage complementary metal oxide semiconductor (LVCMOS) input receivers. Although the SeMI input receivers can digitize the analog timing signals with a low jitter of 10 ps (Won and Lee 2018), the LVCMOS input receivers were used to receive the digital timing signals from a prototype brain PET scanner.

2.2.1. Energy channel.

The energy channel comprises a configurable buffer, non-gated QTC, SeMI input receiver, and multiphase counter (MPCNT), as depicted in figure 3. Dual-channel amplifiers and a double pole double throw (DPDT) switch were used to save space.

The configurable buffer can receive either a differential or single-ended input with both polarities. Two configurable buffers comprised a dual-channel differential amplifier (ADA4932-2, Analog Devices) and a DPDT switch (JS202011CQN, C&K). If the input signal (v_{in}) was positive, the inverting output was selected as the QTC input. If v_{in} was negative, the non-inverting output was selected.

The non-gated QTC converted i_{in} into a dual-slope pulse, which has a pulse width proportional to the input charge. Two non-gated QTCs comprised a dual-channel amplifier (AD8066, Analog Devices), two Schottky diodes (1PS10SB82, NXP), an eight-channel DAC (LTC2625, Linear Technology), and a few passive components. Four QTC channels corresponding to a block detector shared one of eight-channel DAC outputs.

The v_{in} was buffered and linearly converted into the i_{in} using the differential amplifier and a QTC-input-side resistor (R_{in}). The input differential voltage v_{in} was amplified by a closed-loop gain of R_f/R_g , and the output differential voltage (i.e. the voltage difference between positive and negative output nodes)

Table 1. Design values for the energy channel.

Component	Value
Feedback resistor (R_f)	1 k Ω
Gain resistor (R_g)	1 k Ω
QTC-input-side resistor (R_{in})	24 Ω
Feedback capacitor (C_f)	200 pF
Discharge-side resistor (R_{disch})	1 k Ω
Voltage dividing resistors (R_{os} and R_{ot})	50 Ω
DAC voltage output (V_{DAC})	From 1 to 2 V
Constant discharge current (I_{disch})	From 1 to 2 mA
Reference voltage (V_{REF})	-0.1 V
LSB of multiphase counter	625 ps

was $v_{in} \times (R_f/R_g)$. The output common voltage was ground and either positive or negative output voltage of $\pm(v_{in}/2) \times (R_f/R_g)$ was connected to the integrator through R_{in} . Because the inverting input of the integrator was at the virtual ground, the voltage output of the differential amplifier and the DAC voltage output (V_{DAC}) were converted into i_{in} and I_{disch} using R_{in} and a discharge-side resistor (R_{disch}) as in equations (1) and (2), respectively.

$$i_{in} = \frac{v_{in}}{2 \times R_{in}} \times \frac{R_f}{R_g} \quad (1)$$

$$I_{disch} = \frac{V_{DAC}}{R_{disch}} \quad (2)$$

Table 1 summarizes the design values for the energy channel. The pulse width was measured using an MPCNT with a least significant bit (LSB) of 625 ps.

2.2.2. Timing channel.

The timing channel was a heterogeneous sampling tapped-delay-line TDC implemented in the same FPGA (Won and Lee 2016). The coarse counter was a 12-bit binary counter operating at the main clock frequency of 400 MHz and provided the coarse count N . The fine time interpolator consisted of a 256-tap carry chain, sampling flip-flops, a fine code encoder, and a fine time calibrator. The LSB of the TDC was 10 ps. The asynchronous timing signal was delayed with changing the states of the delay elements, after which the states of the delay elements were sampled by the flip-flops at the rising time of the main clock signal. The sampled states were converted into a fine code using a fine code encoder. The fine code was calibrated to a fine time f , for which the dynamic range was from 0 to 2500 ps, using a fine time calibrator. The timing t_{arr} was calculated as in equation (3).

$$t_{arr} = N \times 2500 \text{ ps} - f \quad (3)$$

2.3. Prototype brain PET scanner

The QTC/SeMI DAQ system was applied to the prototype high-resolution brain PET scanner, as depicted in figure 4(a). The prototype scanner consists of 14 detector sectors and has an inner diameter of 254 mm; it can be equipped up to two block rings to yield an axial length of 54 mm. However, a single block ring with an axial length of 26 mm was utilized in this study.

2.3.1. Block detector.

The single block ring comprises 28 block detectors. A high-resolution stacked DOI PET detector comprises a dual-layer crystal block (Sichuan Tianle Photonics Co., Ltd) coupled with a silicon photomultiplier (SiPM) array, as depicted in figure 4(b). The upper layer was a 13×13 array of $1.78 \times 1.78 \times 8 \text{ mm}^3$ lutetium oxyorthosilicate (LSO) crystals, and the lower layer was a 14×14 array of $1.78 \times 1.78 \times 12 \text{ mm}^3$ LSO crystals. All the crystal surfaces were mechanically polished. The crystals were optically isolated using an enhanced specular reflector (ESR, 3 M) film except for the exit face, and the crystal pitches for the crystals of both the layers were 1.86 mm.

The crystal block was coupled with a 2×2 array of 4×4 SiPMs (S13361-3050NE-04, Hamamatsu Photonics K. K.). Optical grease (BC-630, Saint-Gobain) was used to improve the optical coupling between the crystal block and the SiPM array. The cross-sectional area of the block detector was $26 \times 26 \text{ mm}^2$.

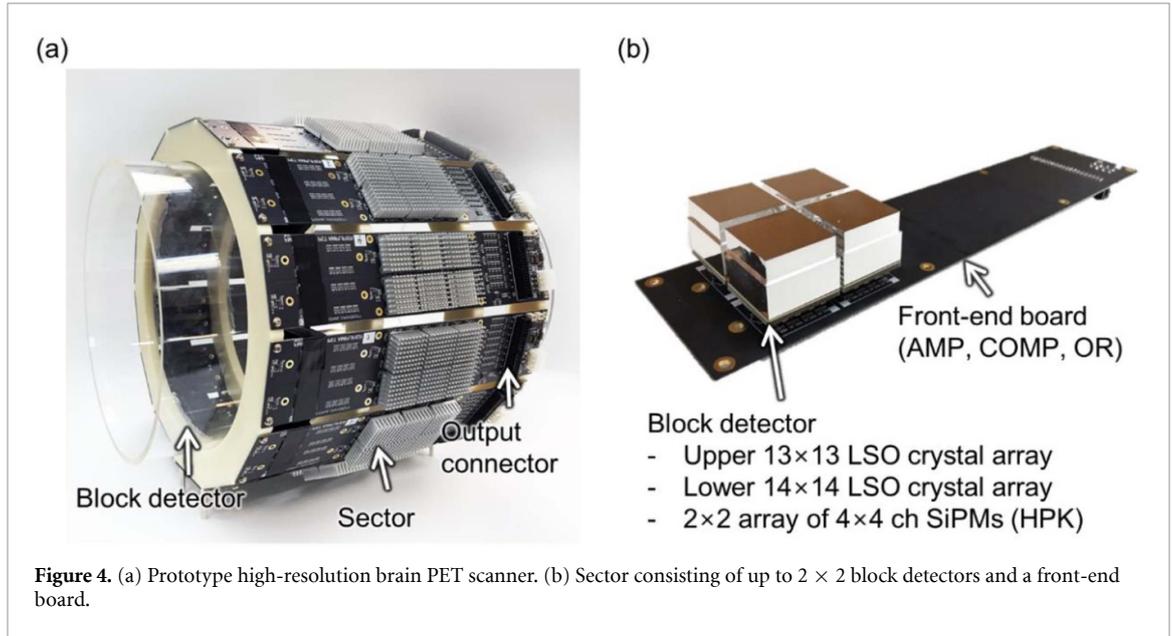


Figure 4. (a) Prototype high-resolution brain PET scanner. (b) Sector consisting of up to 2×2 block detectors and a front-end board.

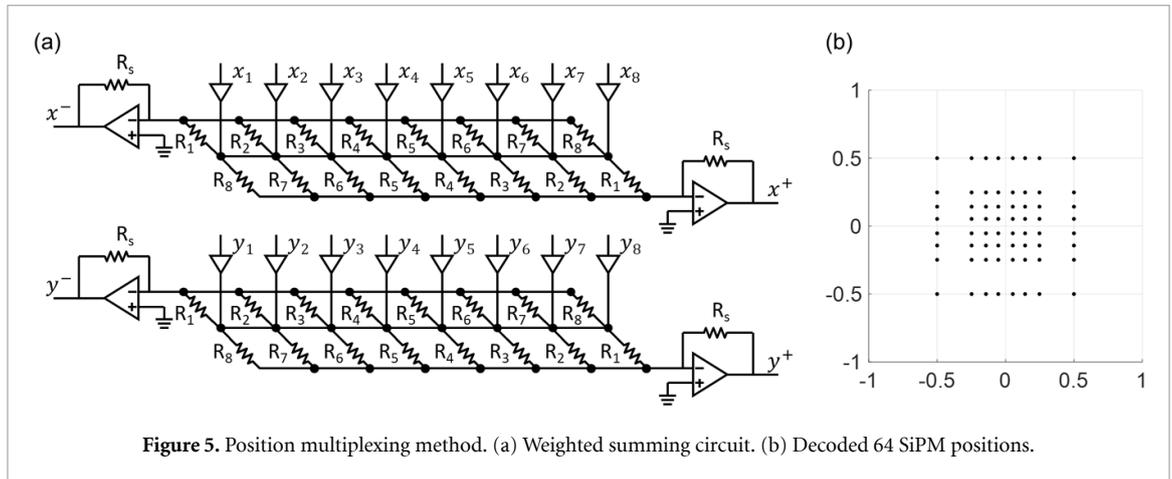


Figure 5. Position multiplexing method. (a) Weighted summing circuit. (b) Decoded 64 SiPM positions.

2.3.2. Sector.

Each sector consisted of 2×1 block detectors and a front-end board (FEB), as illustrated in figure 4(b). The FEB multiplexed the SiPM signals into energy and timing signals. Each output signal from 64 SiPM anodes of the block detector was split into two signals via $50\text{-}\Omega$ resistors and tied together in each row and column direction using amplifiers (AD8003, Analog Devices) (Kwon and Lee 2014). The eight row and eight column signals were then further multiplexed into the four position-encoded energy signals of x^+ , x^- , y^+ , and y^- using weighted summing circuits with weights w_1 to w_8 , as illustrated in figure 5(a). The i -th weight w_i is inversely proportional to the i -th weight resistor value R_i . The x^+ and x^- were calculated using equations (4) and (5). The same w_i and R_i were applied to y^+ and y^- . The multiplexed 64 SiPM positions \hat{x} and \hat{y} were decoded from the energy signals E_{x^+} , E_{x^-} , E_{y^+} , and E_{y^-} using equations (6) and (7), as shown in figure 5(b) and table 2. The weights for the outermost SiPMs were higher than the rest to resolve corner and edge crystals in the flood map more clearly.

$$x^- = - \sum_{i=1}^8 \frac{R_s}{R_i} x_i = - \sum_{i=1}^8 w_i x_i \quad (4)$$

$$x^+ = - \sum_{i=1}^8 \frac{R_s}{R_{9-i}} x_i = - \sum_{i=1}^8 w_{9-i} x_i \quad (5)$$

Table 2. Design values for the weighted summing circuit.

Row signal (x_i)	x^- -side weight resistor (R_i)	x^+ -side weight resistor (R_{9-i})	x^- -side weight (w_i)	x^+ -side weight (w_{9-i})	Decoded position (\hat{x})
x_1	1 k Ω	3 k Ω	1.00	0.33	-0.500
x_2	1.5 k Ω	2.49 k Ω	0.67	0.40	-0.248
x_3	1.65 k Ω	2.2 k Ω	0.61	0.45	-0.143
x_4	1.8 k Ω	2 k Ω	0.56	0.50	-0.053
x_5	2 k Ω	1.8 k Ω	0.50	0.56	+0.053
x_6	2.2 k Ω	1.65 k Ω	0.45	0.61	+0.143
x_7	2.49 k Ω	1.5 k Ω	0.40	0.67	+0.248
x_8	3 k Ω	1 k Ω	0.33	1.00	+0.500

$$\hat{x} = \frac{E_{x+} - E_{x-}}{E_{x+} + E_{x-}} \quad (6)$$

$$\hat{y} = \frac{E_{y+} - E_{y-}}{E_{y+} + E_{y-}} \quad (7)$$

In addition, eight column signals were fed into the respective comparators (ADCMP601, Analog Devices), and the logic outputs of the comparators were then OR-ed to generate a single digital timing pulse. The multiplexing ratios for the energy and timing signals were 64:4 and 64:1, respectively. A total of 16 energy and four timing signals were output per sector.

A microcontroller unit (ATmega128A, Atmel) controlled the DAC (AD5629R, Analog Devices) outputs using an inter-integrated circuit (I²C) interface to adjust the SiPM bias voltages and the comparator threshold voltages. The SiPM bias voltage of the block detector was set at 30 times the DAC output using a bias controller (ADL5317, Analog Devices).

2.4. Data acquisition chain

Two QTC/SeMI DAQ systems were used to collect data from the prototype PET scanner. The signals from the six sectors were fed into the first DAQ system, and the other signals from the eight sectors were fed into the second DAQ system through 40-pin ribbon cables. The two QTC/SeMI DAQ systems and a master DAQ were connected using a daisy chain through a gigabit transceiver with the line rate of 2.5 Gbps. A pair of coaxial cables were used for data transmission.

The master DAQ was implemented using a Virtex-6 evaluation kit (ML605, Xilinx). It identified the prompt and delayed coincidence events based on the timestamps and transmitted them to the computer through 1 Gbps Ethernet (Son *et al* 2017b).

The two QTC/SeMI systems were synchronized using two in-house clock distributors. The clock distributors consisted of a 2:8 clock fanout buffer (8SLVD1208, IDT) and a 200 MHz clock oscillator (SiT9120, SiTime). One clock distributor was used to feed the common clock signals, and the other was used to feed the synchronization signals.

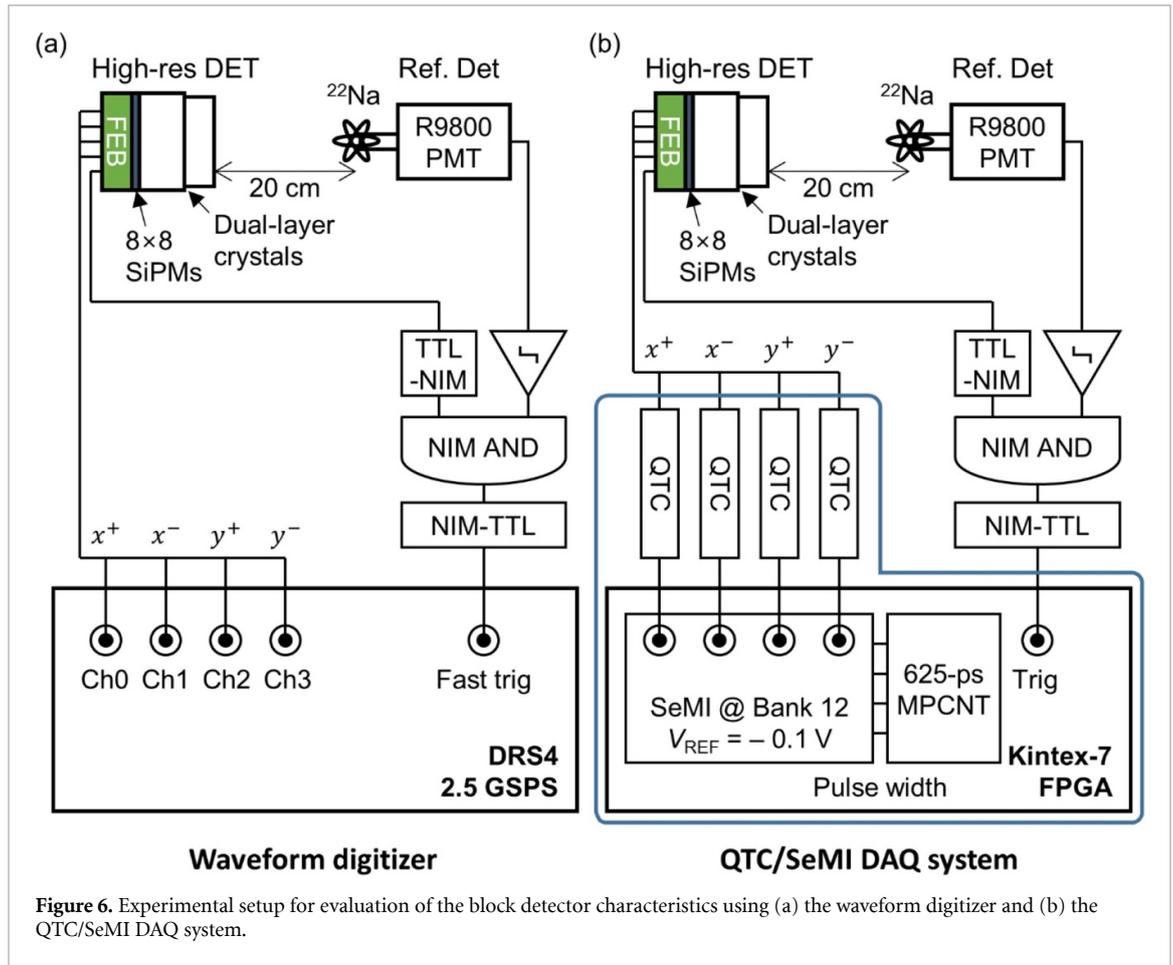
2.5. Experimental setup and data processing

2.5.1. Energy linearity.

The energy linearity of the energy channel was evaluated by applying the exponential pulses (v_{exp}) with different amplitudes to the energy channel using a digital detector emulator (DT5800D, CAEN). The 10%–90% rise and decay times of v_{exp} were 7 ns and 40 ns, respectively. The peak amplitudes were swept from 0.6 to 3.3 V in steps of 0.3 V. I_{disch} was 2 mA. The pulse width when v_{SeMI} was higher than V_{REF} was measured. The pulse widths of v_{SeMI} for 10 240 test pulses were measured and the mean and full width at half maximum (FWHM) were evaluated.

2.5.2. Evaluation of block detector characteristics.

The signals from the block detector were digitized using a waveform digitizer (DT5742B, CAEN) and the QTC/SeMI DAQ system to verify that the QTC/SeMI DAQ has a comparable DAQ performance with that of the waveform digitizer, as illustrated in figure 6. A reference detector (R9800, Hamamatsu Photonics K. K.) and nuclear instrument modules (NIMs) were used to obtain the coincidence events. A ²²Na point source was attached to the reference detector, and the distance between the block detector and the reference detector



was 20 cm. The timing pulse of the block detector was converted to the NIM trigger using a NIM-TTL-NIM adapter (N89, CAEN) and then fed into a coincidence module (N455, CAEN). The timing pulse of the reference detector was generated using a discriminator module (N843, CAEN), and then fed into the coincidence module. The coincidence trigger was fed into the NIM-TTL-NIM adapter, and then converted into a transistor-transistor logic (TTL) interface. Both the waveform digitizer and the QTC/SeMI DAQ system collected 2 000 000 coincidence events.

2.5.2.1. Experimental setup and data processing using the waveform digitizer.

In the experimental setup using the waveform digitizer depicted in figure 6(a), the coincidence trigger was fed into a fast trigger of the waveform digitizer. In addition, four energy signals were fed into the waveform digitizer. The waveform digitizer sampled the energy signals with a sampling rate of 2.5 giga-sample per second (GSPS) and a resolution of 12 bits. The energy signals of x^+ , x^- , y^+ , and y^- were accumulated for 140 ns after the respective baseline correction, and the respective energy values of E_{x^+} , E_{x^-} , E_{y^+} , and E_{y^-} were obtained. The crystal positions \hat{x} and \hat{y} were calculated using equations (6) and (7), respectively. The energy E was calculated using equation (8).

$$E = \frac{E_{x^+} + E_{x^-} + E_{y^+} + E_{y^-}}{4} \quad (8)$$

We used a flood quality parameter of a distance-to-width ratio (DWR) using the concept of k -parameter (Du et al 2013). The DWR value of the i -th upper-layer crystal between four adjacent lower-layer crystals was calculated using equation (9).

$$DWR_i = \frac{1}{8} \sum_{j=1}^4 \left(\frac{x_i - x_j}{(w_{x,i} + w_{x,j})/2} + \frac{y_i - y_j}{(w_{y,i} + w_{y,j})/2} \right) \quad (9)$$

In equation (9), x_i , y_i and x_j , y_j are the x and y positions of the i -th and j -th crystals in the flood map, respectively. $w_{x,i}$, $w_{y,i}$ and $w_{x,j}$, $w_{y,j}$ are the FWHM of 1D profiles along the x and y directions of the i -th and

Table 3. Experimental setup and reconstruction parameters for phantom studies.

	Hot-rod phantom	Uniform phantom	Brain phantom
Initial activity (mCi)	1.3	1.7	1.7
Scan time (hours)	2	2	2
Total number of prompt coincidences	990 M	140 M	671 M
Iteration number	64	2	32
Number of subsets	4	4	4
Voxel size (mm ³)	0.465 × 0.465 × 0.93	0.93 × 0.93 × 0.93	0.93 × 0.93 × 0.93
Gaussian post-filter kernel size (mm)	0.93	—	1.86

j -th crystals, respectively. A larger DWR indicates that the crystals are more clearly resolved. The mean and standard deviation (STD) values of DWR were expressed as mean ± STD.

The global energy spectrum and energy resolution value before crystal identification were obtained. In addition, the per-crystal energy photopeak positions and energy resolutions were evaluated after crystal identification. The energy resolution value was expressed as the FWHM of the Gaussian function.

2.5.2.2. Experimental setup and data processing using the QTC/SeMI DAQ system.

In the experimental setup using the QTC/SeMI DAQ system depicted in figure 6(b), the coincidence trigger was fed into the trigger channel. The energy signals were digitized by four energy channels, and the measured pulse widths were considered to be the energy values of E_{x+} , E_{x-} , E_{y+} , and E_{y-} . The crystal positions and energy were calculated using equations (6)–(8), as performed with the waveform digitizer. The DWR values, per-crystal photopeak positions, and energy resolutions were also evaluated and compared with those obtained using the waveform digitizer.

2.5.3. Phantom studies.

Hot-rod, uniform, and two-dimensional (2D) Hoffman brain phantoms were imaged using the PET scanner and the QTC/SeMI DAQ systems. The hot-rod phantom had six types of hot rods, with diameters of 1.2, 1.6, 2.4, 3.2, 4.0, and 4.8 mm. The uniform phantom had an inner diameter of 10.8 cm. An energy window of ±20% of the photopeak and a timing window of ±2 ns were applied.

All phantoms were filled with ¹⁸F-fluorodeoxyglucose (¹⁸F-FDG), and the phantom images were reconstructed using in-house software. The detailed experimental setup and the reconstruction parameters are summarized in table 3.

The PET image reconstruction and corrections were performed using our in-house software and processing pipeline that have been also applied in our previous works (Ko *et al* 2016b, Lee *et al* 2017, Son *et al* 2017a, Hwang *et al* 2018). The reconstruction method was a line-of-response ordered subset expectation maximization (LOR-OSEM) (Kadrmas 2004) using a distance-driven projector (Man and Basu 2004). All components in the system response matrix were derived from the geometry of line-of-response which is determined by the center position of each crystal. The two-layer DOI information was used to calculate the system response matrix without compression or re-binning, which provided more precise sampling than DOI compression to a single layer. The number of LORs between upper- and upper-layer crystals, upper- and lower-layer crystals, lower- and lower-layer crystals were 8 796 788, 20 404 384, and 11 832 128, respectively. The LORs between 28 block detectors in 14 sectors and 22 block detectors in 11 opposite sectors were used for reconstruction.

The normalization factors were measured using data obtained with a ⁶⁸Ge quality assurance cylindrical phantom source. The attenuation correction factors were obtained using the x-ray CT scans co-registered with uncorrected PET images. The random correction using the delayed coincidence data acquired by the coincidence processor was applied. The scatter correction was not applied.

We measured the peak-to-valley ratio (PVR) value of hot-rod phantom and the uniformity (%STD) of the uniform phantom using equations (10) and (11), respectively. N_h is the number of examined hot rods. $I_{v,i}$ is the image intensity of the i -th valley. $I_{p,l,i}$ and $I_{p,r,i}$ are those of two nearest peaks. I_{ROI} is the image intensity of the region of interest (ROI).

$$PVR = \frac{1}{N_h} \sum_{i=1}^{N_h} \left(\frac{I_{p,l,i}}{I_{v,i}} + \frac{I_{p,r,i}}{I_{v,i}} \right) / 2 \quad (10)$$

$$\%STD = \frac{STD(I_{ROI})}{Mean(I_{ROI})} \times 100 \quad (11)$$

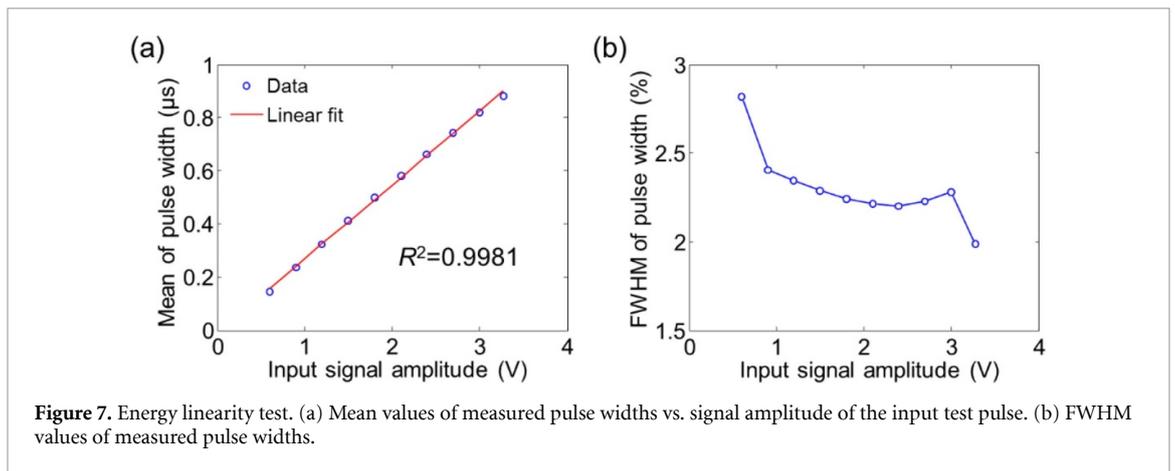


Figure 7. Energy linearity test. (a) Mean values of measured pulse widths vs. signal amplitude of the input test pulse. (b) FWHM values of measured pulse widths.

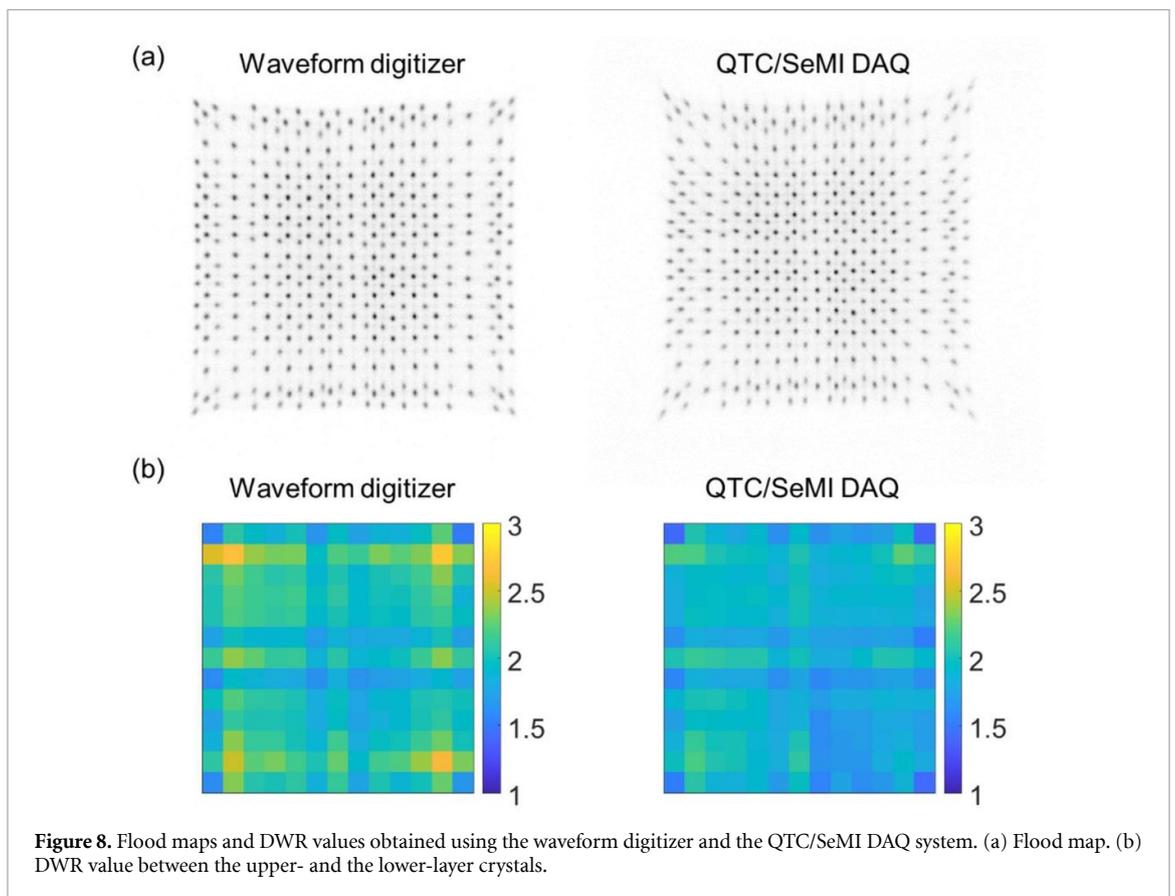


Figure 8. Flood maps and DWR values obtained using the waveform digitizer and the QTC/SeMI DAQ system. (a) Flood map. (b) DWR value between the upper- and the lower-layer crystals.

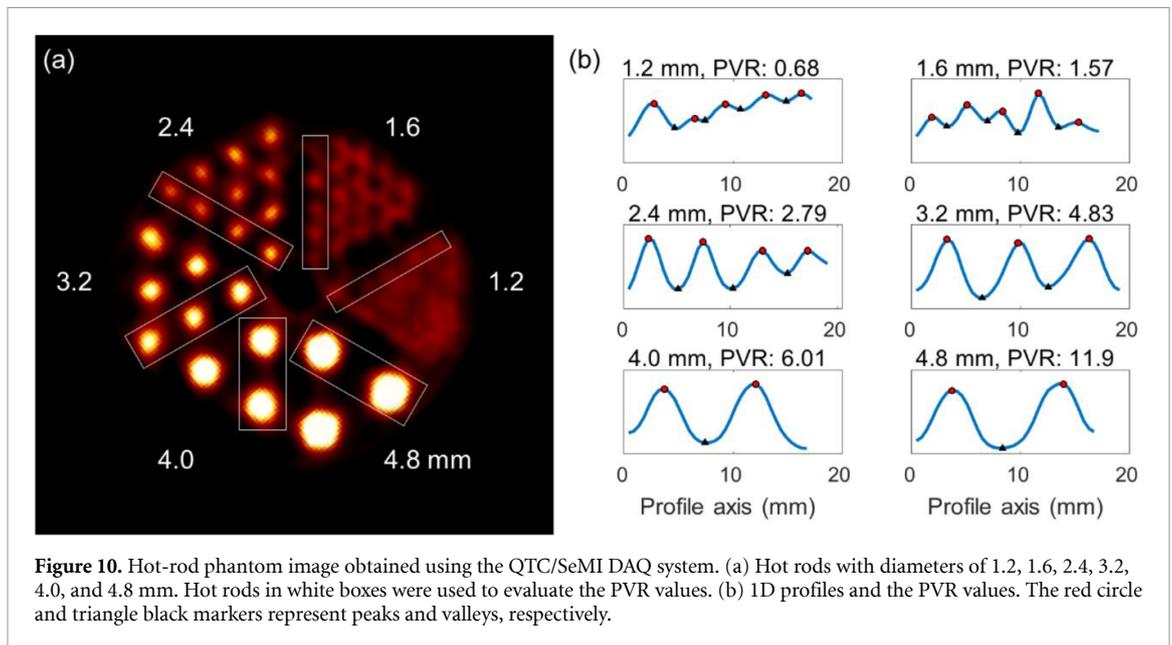
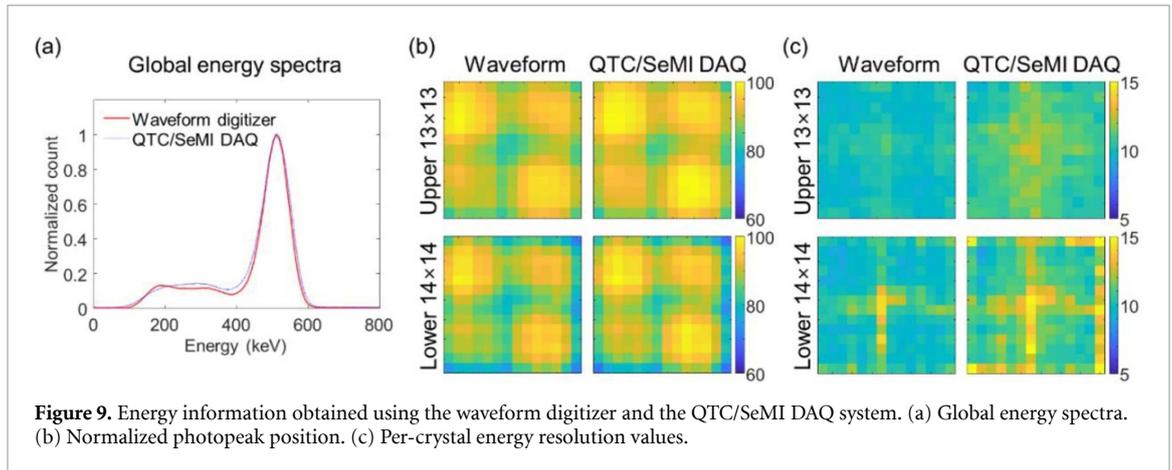
3. Results

3.1. Energy linearity

The pulse width of the modulated exponential pulse changed linearly with the amplitude of the exponential pulse. A linear fit was applied to the measured data and the R-squared (R^2) value was 0.9981, as depicted in figure 7(a). The FWHM value of the pulse width was less than 3%, as depicted in figure 7(b).

3.2. Evaluation of block detector characteristics

Figure 8 illustrates the flood maps and the DWR values obtained using the waveform digitizer and the QTC/SeMI DAQ system. For both DAQ systems, all crystals of the two crystal layers were clearly resolved in the flood maps. This indicates that four energy channels of the QTC/SeMI DAQ system can decode the position information of the high-resolution crystals with small pitches of 1.86 mm and dual-layer DOI information.



The DWR values were 2.03 ± 0.21 and 1.85 ± 0.15 for the waveform digitizer and the QTC/SeMI DAQ system, respectively. The flood map obtained using the SeMI/DAQ system was slightly degraded, especially for the corner crystals with a low input charge to one of the four QTCs.

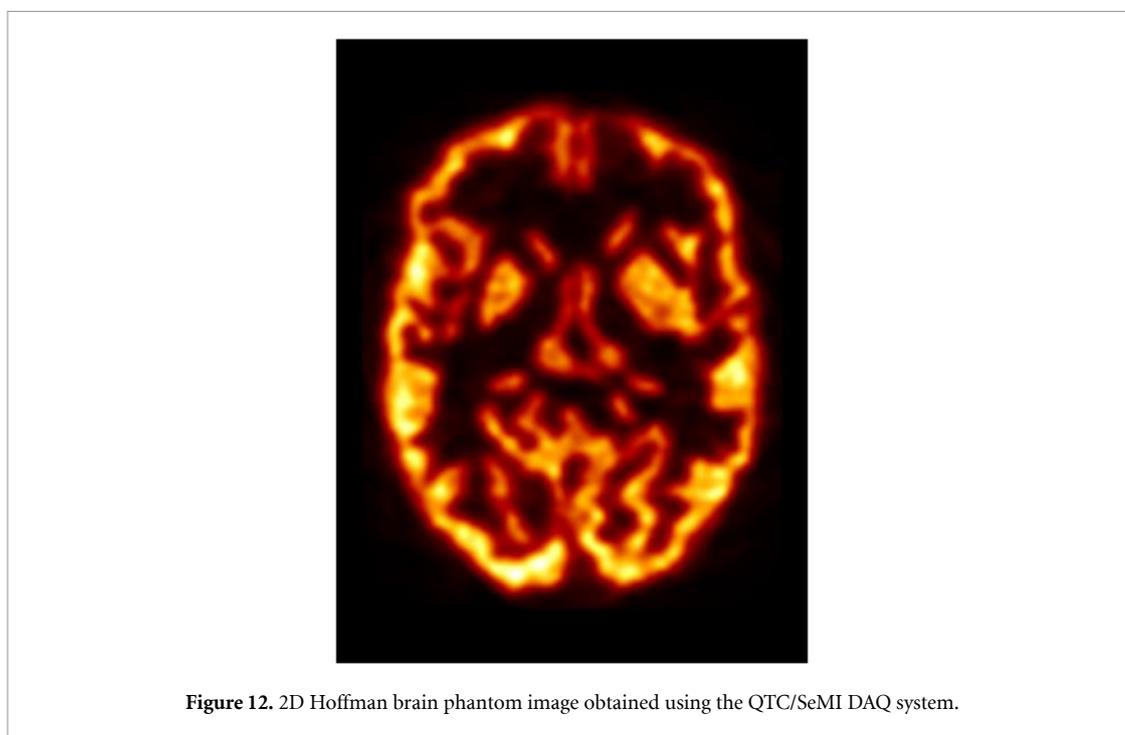
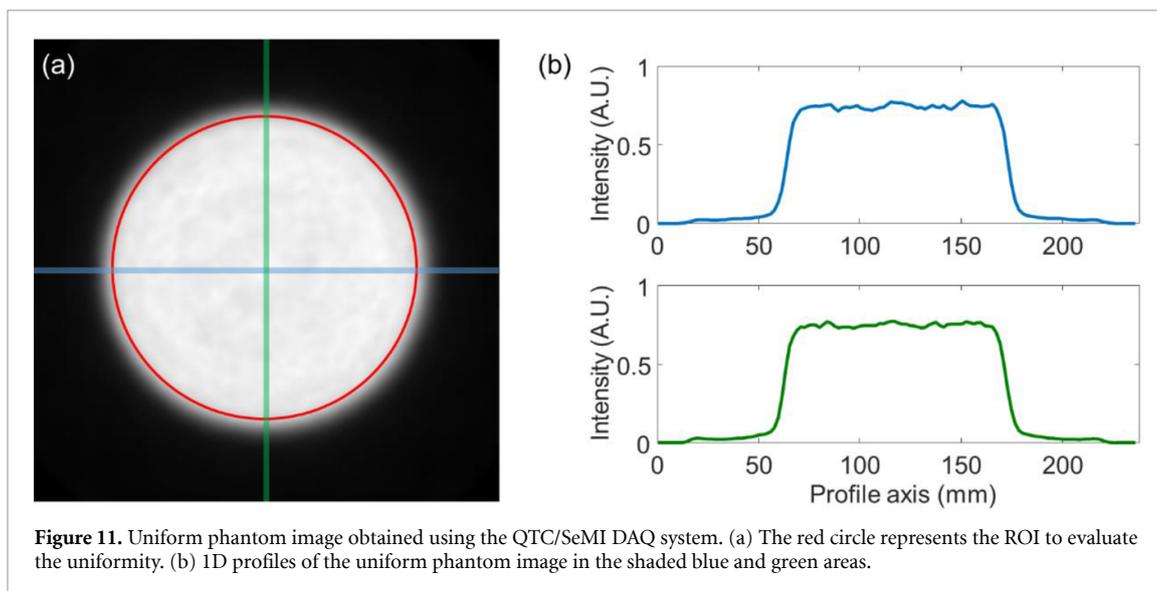
The energy spectra of the block detector obtained using the waveform digitizer and the SeMI/DAQ system were almost identical, as depicted in figure 9(a). The energy resolution values before the crystal identification were 17.0% and 18.4% for the waveform digitizer and the QTC/SeMI DAQ system, respectively. The dual-slope pulse width corresponding to 511 keV photon was 670 ns for the QTC/SeMI DAQ system.

The normalized per-crystal photopeak positions were almost identical for the waveform digitizer and the QTC/SeMI DAQ system, as depicted in figure 9(a). The per-crystal energy resolution values were slightly degraded, especially in the lower-layer corner crystals, as depicted in figure 9(b). The energy resolution values for the upper and lower layers obtained when using the waveform digitizer were $9.9 \pm 0.4\%$ and $10.2 \pm 0.9\%$, respectively, and those obtained using the QTC/SeMI DAQ system were $11.0 \pm 0.6\%$ and $11.4 \pm 1.4\%$, respectively.

3.3. Phantom studies

The hot rods with a diameter of 1.6 mm could be resolved in the reconstructed image, as depicted in figure 10. The hot rods in white boxes of figure 10(a) were examined to evaluate the PVR value. The PVR values for hot rods with diameters of 1.2, 1.6, 2.4, 3.2, 4.0, and 4.8 were 0.68, 1.57, 2.79, 4.83, 6.01, and 11.9, respectively, as depicted in figure 10(b).

The uniformity of the phantom image illustrated in figure 11 was 1.82%. In addition, the 1D profiles were uniform within the ROI. The detailed structure of the Hoffman brain phantom was clearly reconstructed, as depicted in figure 12.



4. Discussion

The combination of a QTC with a SeMI input receiver has the advantages of multi-channel signal digitization capability and energy linearity.

The first advantage of the combination of QTC and SeMI input receiver is a simple circuit. The non-gated QTC is a simple electronics that comprises an amplifier, a few passive electronics, and a voltage source. Although the implemented energy channel included a configurable buffer before the non-gated QTC to develop a versatile DAQ system, the configurable buffer is not a mandatory component. In addition, the DAC used as the voltage source can also be replaced with an FPGA output buffer (Sousa *et al* 2004, Zhao *et al* 2017, 2018). The multi-channel DAC has the advantage of an easy adjustment of I_{disch} ; however, it increases the circuit complexity. The FPGA output buffer typically supports the current drive capability of up to 16 mA; thus, eight QTCs with I_{disch} of 2 mA can share one FPGA output buffer. Furthermore, the energy channel implemented in this study is simpler than that of the conventional non-gated QTCs using discrete voltage comparators (Liu *et al* 2010, Parl *et al* 2012). The SeMI input receiver can digitize the non-gated QTC outputs without a discrete voltage comparator and provide a common threshold with zero offset voltage, which is required for a non-gated QTC (Won and Lee 2018). Thus, the 132 energy channels can be

implemented using 137 of the 192 available FPGA I/O ports, that is, 132 and five ports were used for the SeMI input receivers and the common thresholds, respectively.

The second advantage is energy linearity. The non-gated QTC is an integrator that converts the input charge into the pulse width linearly, regardless of the pulse shape. The linear charge measurement capability of the QTC enabled resolving all crystals of the high-resolution stacked DOI PET detectors. Although the spots for edge crystals were blurred in the flood map and the energy resolutions were degraded because of low charge injection to one of the four QTC channels, this can be mitigated by increasing the input current in the energy channel and/or decreasing the charge division ratios in the charge division circuit.

The third advantage is a simple data processing. The pulse width of the dual-slope pulse can be easily measured using the MPCNT without complex pulse reconstruction procedures.

In comparison with the conventional time-based signal digitization method using the FPGA, SeMI digitizers with the ToT method can digitize the detector signals without front-end electronics (Won and Lee 2018); however, they cannot be used to digitize the signals of a block detector with light sharing and charge division circuits because of the energy non-linearity and pulse shape distortion. The FPGA-only digitizers using the MVT method can digitize the signals linearly but suffer from pulse shape distortion resulting from the charge division circuit (Xi *et al* 2013). In addition, the MVT method with four threshold voltages requires eight FPGA I/O ports per energy channel. The 1-bit sigma-delta modulation method can be used to digitize the block detector signals because of the high energy linearity and integrator-based architecture (Zhao *et al* 2017, 2018). The electronics are also simplified using the FPGA I/O ports as a comparator and an output driver. The comparator can be further simplified using SeMI input receivers instead of low-voltage differential signaling (LVDS) input receivers. Each LVDS input receiver requires two FPGA I/O ports, whereas each SeMI input receiver requires one FPGA I/O port.

The limitations of this study are as follows. First, we obtained the phantom images, but we did not fully measure the brain PET scanner performance because the scanner is still under development. In this study, we focused on verifying the concept of a comparator-less QTC and the multi-channel signal digitization capability of the SeMI input receivers. Second, we obtained the system-level coincidence timing resolution of 1.077 ± 0.183 ns with a ^{22}Na point source placed at the center of field-of-view. We will optimize the bias and threshold voltages to improve timing resolution and measure the scanner performance using the NEMA standards in future studies.

5. Conclusions

We developed a comparator-less QTC/SeMI DAQ system consisting of 132 energy and 33 timing channels. The linear FPGA-based charge measurement method of QTC/SeMI was used to implement the energy channel. The non-gated QTC output was directly digitized by the SeMI digitizer. The linear charge measurement enabled resolving all high-resolution crystals of the block detectors with the light sharing and charge division circuits using four energy channels. The multichannel signal digitization capability of the DAQ system was verified by collecting data from the high-resolution brain PET scanner and visualizing the phantom images successfully.

Acknowledgments

This work was supported by grants from the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT (Grant Nos. NRF-2014M3C7034000 and NRF-2016R1A2B3014645) and the Ministry of Education (NRF-2018R1D1A1B07045559).

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